REVIEW

Revolution of optical computing logic gates based on its applications: an extensive survey

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Abstract. Nowadays, communication has grown into a key area with a rapidly growing user community. The existing broadband users are overcrowded, and its faster speed has now become an essential parameter to meet the consumer's expectations in the growing technology. As a result of our growth in computer technologies, high-speed processors are necessary, which provide simultaneous data computing with lower costs and a performance of more than 10,000 times quicker than electrical computers. Optics has become a more feasible alternative to electronics because of its greater speed. In this study, various methods of photonic crystals (PhCs) have been thoroughly examined, with essential properties and their benefits explained over previously identified methods (semiconductor optical amplifier and nonlinear waveguides) utilized to construct all-optical logic circuits. Particularly, evaluated a number of articles that covered topics including self-collimation effects, PhC waveguide intersection, and multi-mode interference with nonlinear effects. The merits and demerits of each technology are analyzed. Finally, concluded the major difficulties and the potential usage of every method. PhCs are used in logic circuits and devices for high data transmission. The performances of different types of logic gates based on PhC are studied. [DOI: 10.1117/1.OE.61.11.110901]

Keywords: interference; multimode interference; nonlinear waveguide; nonlinear Kerr material; semiconductor optical amplifier; self-collimated beam.

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1 Introduction

With the advance of technology, there is a significant change in information technology in many places over the years. Earlier techniques of developing digital computers (1623 to 1945) were the initial means of creating a machine.[1] Scientist attempted to create devices that could readily answer arithmetic problems in the early 17th century. A number of researchers, including Wilhelm Schickard, Blaise Pascal, and Gottfried Leibniz, attempted to develop a calculator that could handle adding, subtracting, multiplying, and dividing. George Schertz and Edward Schertz created a system that can handle 15-digit values using a 4-bit difference engine. The US Bureau Of labor statistics is among the organizations that employed the mechanical computer for card-based technology designed by Herman Hollerith of the Business Development Computers firm for the enumeration.

Due to the mechanical laptop's massive size, sluggish speed, and limited capability and sophistication, quantum computing transitioned to the embedded processor. Instead of electronic control used in mechanical computers, electronically switched in the form of gallium arsenide and used in desktop devices. Researcher JV Standoff made the first effort at building an embedded device, creating a system that resolved system of equations. Konrad Zuse, often regarded as the father of the computing, created the design of the *Z*'1 and *Z*'3 computed systems in Berlin around 1936 and 1941.[2] However, the change of time, it led to the development of smaller desktop devices with faster speed, easy fabrication with less heat loss. As a result, vacuum tube-based electrical switches were substituted by diode and semiconductor innovation,

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which has a switching time of 0.3 μs. Transistor digital computer, developed by Bell Telephone laboratories in 1954, was the very first machine draught to use this approach.[3] However, semiconductor technology execution was still sluggish and limited to a single application. Integrated circuits (ICs), included semiconductor devices with a significant number of components on an IC. microelectronics recollection, and micro programming were developed to tackle the restrictions of light-emitting diodes and power amplifier technology. They became a basic technical requirement for quicker and more effective methods for integrating multiple processing power.[4]

Small-scale integrating circuits, which contain roughly had 10 components per circuit, were used in the earlier ICs, which expanded into middle-scale IC, that have up to 100 units per chip. In 1972, major integrates (1000 gadgets) and very sizable integration technologies are evolved, which utilized to build electric systems with the benefits of fast computing speed with precision, small footprint receiving increasing attention. To date, the lowest scale achievable with VLSI technology has been 0.09 mm.[5]

However, in today's form of global networks and activities, such as online video and entertainment, there is a desire for processors with high speed, simple structure, reduced size, and greater precision with less amount of heat loss. Optics is the greatest potential answer for meeting these requirements since it provides an accurate and faster way of transmitting information from one location to the next. This is due to the fact that a laser source can readily pass through an open space without encountering any reverberation. Optics offers a way to push the frontiers of ultrafast data transfer while saving money and increasing dependability. As a result, the optical computing is the greatest alternative to the electrical computer since it can do many processes at once and analyze information 100,000 times quicker.[6] Another benefit of optics versus transistors is full throttle minimal thermal management. The most commonly cited benefit of optical computers is efficiency. Electronics typically employ either time or space to handle complexity, but optics provides a third technique fan in and fan out. A single pixel in an optical processing may modify several separate beams. Another factor is heat absorption in electrical gadgets, which is moderated by optics as speed grows.[7] So, according to Moore's law (doubling the transistor density every two years), as time passes, the density decreases, which is moderated by optics.

An additional benefit of optics is that the message may be conveyed without voltage since the created light follows wave equations and propagates on its own. Spectrometers are also small, light, and cost-effective. Fiber, diamonds, and semiconductors are combined to develop an optical processor that will be 100 million users speed than currently available devices by substituting particles with the photon. A wide range of hardware, such as optical gates, optoelectronic devices, optical connections, and optical memories are required to form an optical computing device.

The applicability in ultrafast cognitive processing and the capacity to carry out various logical functions in optical computing environments, all-optical circuits have become progressively prevalent. As a result, creating all-optical logic circuits is the first phase for realizing complicated digital functionality in optical computing.[8] Electronic ICs were previously employed, but the highest switching speed obtained was 50 ps with a common output power of 0.5-mW per switch. The limited inductance of $p-n$ junctions in semiconductor-based logic circuits is the explanation behind this.[9] Despite the capacitor, the duty cycle of photonic logic circuits is in the nanosecond range and is now only constrained by the light ray traveling through them.[10] The design of all optical logic gates can be expressed in a variety of methods. The first technique employs a semiconductor optical amplifier (SOA), which has a high gain owing to reflection index variations.

Cross-phase attenuation, four-wave mixing, and cross-gain modulation, are some of the techniques used.[11] SOA was also utilized to construct metadata emotional and social support gates, which are all-optical logic gates.[12] However, metadata gates have a number of drawbacks, including SOA-based devices being limited by SOAs slow carrier time to recover, unstable gates because of polarization sensitivity, and Mach–Zehnder interferometer (MZI) strategy,[13] which demands one or more SOA and complicates the framework by requesting the correct configuration of the filtration of SOAs with the help of optic fiber logic circuits, as the pattern of the riddle diminishes the ratio of noise.[14] Nonlinear diffraction gratings, in which localized nonlinear medium were used by altering the current power, are just another way for constructing all-optical logic gates. Many drawbacks of asymmetric logical gates exist, notably as the need for high

pressures signal power and polarization independence, which pose production issues.[15] Despite the fact that today's embedded integrated barriers are compact, switching is still constrained.

We believe that photonic crystal (PhC)-based optical gates are the only way to address the drawbacks of the preceding methodologies. These would be discussed in depth in this study, and they are divided into bandwidth-based gates and non-bandwidth-based gates. The main factors evaluated and analyzed were area ($\mu m \times \mu m$), bit rate (Tb/s), contrast ratio (CR-dB), and tolerance value.

2 PhC-Based Logic Gates

PhCs are occasionally constructed electromagnetic medium with photon direct bandgaps that prevent light from propagating through them. John[16] was the one who invented PhC. Unlike semiconductor crystals, which alter the characteristics of electrons; those crystals impact the property of light. Light has various benefits over electrons, including the ability to move faster in piezoelectric medium than ions in metallic wire and has larger capacity in the dielectric medium than electons. The capacity of fiber-optic communication devices is on the range of 1 THz, whereas throughput of computer equipment is on the level of few thousand hertz. PhCs provide a regular piezoelectric medium for light to pass through, with fluctuations in both directions. So, a PhC is classified as contributed to the understanding on the orientations in which it may give periodical fluctuations in dielectric medium.[17]

1. One-dimensional (1D) PhCs: structural features with only one manner of insulating main stream variation in one direction;
2. Two-dimensional (2D) PhCs: structural features with dielectric main stream with different variants in two directions; and
3. Three-dimensional (3D) PhCs: structural features with dielectrics having different variants in three different directions.

As shown in Fig. 1, a 1D PhC is a form of crystal that exhibits periodic dielectric environment fluctuations only with 1D Fig. 1(a). Antireflection reflectors as the primary rear view mirror in automobiles, translucent TV displays, and more uses for 1D PhCs. However, 1D PhCs have limited uses and could be utilized to produce all-optical logic circuits since this needs light confinement, which is only possible with 2D and 3D PhCs.

As shown in Fig. 1, 2D PhCs provide a periodical piezoelectric fluctuation in two different directions to the flow of photon Fig. 1(b). These crystals are commonly utilized to produce all-optical logic circuits in situations with various flaws, such as self-collimated beams, MZIs interruption, and non-linearity.

As shown in Fig. 1, the 3D PhC enables dielectric medium modifications in all 3D Fig. 1(c). They localize light to the center of the PhCs, 3D PhCs are more sophisticated than other forms of PhCs. The photonics bandgap (PBG), which would be equivalent to the absorption edge of crystalline molecular framework, is present in all PhC dielectric configurations (1D, 2D, and 3D). The bandgap is a frequency range that is not allowed to travel in the structure of the crystal.

Only absolute symmetry in the PhC structure allows for a perfect absorption edge. By adding imperfections in the crystalline lattice, light from certain wavelengths may be made to pass

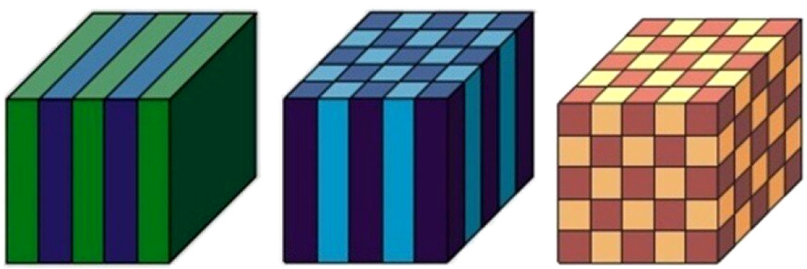

Fig. 1 Waveguide regularity: (a) regularity in 1D; (b) regularity in 2D; and (c) regularity in 3D.[18]

through it. It can regulate the flow of electrons or magnetic fields with the aid of a PBG. One of the most significant functions in the realm of high transmitting data that 2D PhCs may achieve is all-optical physical devices. Furthermore, there are two kinds of PhC-based gates: bandgap and non-bandgap.

3 Optical Logic Gates based on Non-bandgap

Instead of identifying the bandgap of the devices, the incoming light of various wavelengths is given at the output, and a logical operation is conducted by means of a self-magnified image light in non-bandgap–based PhC gates. In this case, incoming light continues to perpetuate in a structure at a given direction without diffraction. The characteristic of total internal reflection (TIR) is utilized to construct all-optical logic gates utilizing a self-collimated photon. TIR dependent on the approach of incident is greater than the standard angle, as per the relation $\theta >$ arc sin (n_L/n_H), where n_L represents the low dielectric constant and n_H represents the high absorption coefficient. Figure 2 illustrates the mechanism to see how the self-collimated laser works.

4 Operation Principle and Analysis of Structure

A photonic-integrated circuit (PIC) device is active and self-collimated in a 2D PhC were planned in Ref. 19. The gadget was useful for making optical switch and logical gates, and both are important parts of a PIC. The construction with Si rods in air was designed using square lattice architecture. The suggested structure's radii and dielectric characteristics were determined to be $r = 0.36a$ and $\varepsilon = 13$, respectively. By lowering the dimension of $0.275a$, a line fault in the x direction was generated to transfer the laser. Due to the symmetry of the device, low index gap has the amplitude of transmission $te^{i\varphi}$, so the amplitude of reflection is $re^{i(\varphi+\Pi/2)}$. The idea was to make a medium with a low-refractive indices such that one portion of the beams could continue to travel while the other was reflected, indicating the position of an object. By altering the time delay between the reflected light beams, the OR and XOR gate structures were developed. When the phase difference here between incoming beams was $2k\Pi + \Pi/2$, output O_1 behaved as an XOR gate and outputs $O2$ as an OR gate, as shown in Fig. 2. When the phase difference was $2k\Pi - \Pi/2$ owing to a difference of $-\Pi/2$ seen between input lasers, from the other hand, output O_1 worked as an OR logic and $O2$ as an XOR logic. The beams O_1 and O_2 can be written as a linear configuration of transmitted and reflected beams. The structure in Fig. 2(a) has four faces. (I_1, I_2) as the input faces and (O_1, O_2) as the output faces. Before passing the self-collimated beams to investigate the functions of logic gates, reflected and transmitted beams phase shift should be known.

The average refractive index difference in the region of defect (green region) is lower when compared with the other surrounding regions. It is a lossless beam splitting system with a phase difference of $\Pi/2$. The rod radii of the line defect is very less than the other surrounding rods and hence the reflected beams has a phase lag of $\Pi/2$ when compared to the beams transmitted.

Suppose the input incident rays I_1 and I_2 has a beam field of $E1 = vEe^{-i\varphi 1}$ and $E2 = vEe^{-i\varphi 2}$, where $\varphi 1$ and $\varphi 2$ are real, E denotes a plane wave and v is a function of same

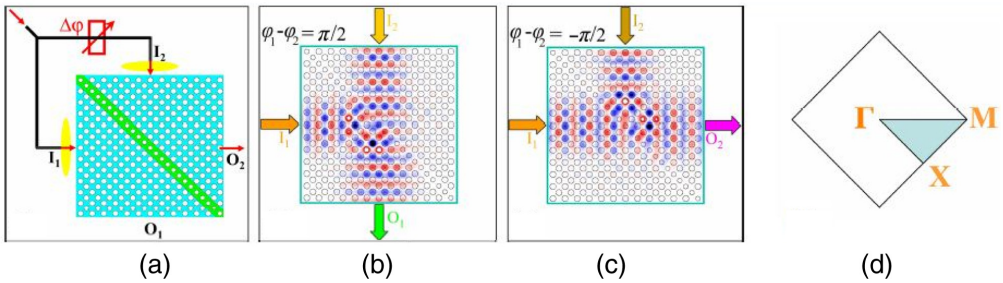

Fig. 2 (a) The square lattice construction for XOR and OR logic with phase shifter;[19] (b) when phase difference is $\Pi/2$; (c) when phase difference is $-\Pi/2$; and (d) various orientations.

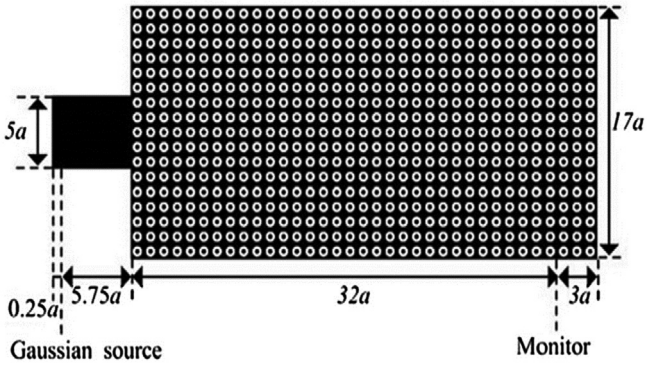

Fig. 3 Optoelectronics diffraction pattern for SC interferometer,[20] whereby white is the concentric circle with radius R and orange is the interior ring with radius r.

periodicity with PhC. There is phase difference between the two incident rays. The transmitted rays and the reflected rays of the two incident beams can be expressed as

$$T_{\mathrm{I1}} = E_1.te^{i\varphi} = v\,Ee^{-i(\varphi 1-\varphi)}\sqrt{2}, \tag{1}$$

$$R_{I1} = E_1.\mathrm{re}^{i(\varphi+\Pi/2)} = v\,Ee^{-i(\varphi 1-\varphi-\Pi/2)}\sqrt{2}, \tag{2}$$

$$T_{\mathrm{I2}} = E_2.te^{i\varphi} = v\,Ee^{-\mathrm{i}(\varphi 2-\varphi)}\sqrt{2}, \tag{3}$$

$$R_{I2} = E_2.\mathrm{re}^{i(\varphi+\Pi/2)} = v\,Ee^{-i(\varphi 2-\varphi-\Pi/2)}\sqrt{2}. \tag{4}$$

The output beams O_1 and O_2 is a combination of transmitted and reflected beams,

$$\begin{aligned} O_1 &= R_{I1+}T_{I2}, \\ &= v\,Ee^{-i(\varphi 1-\varphi-\Pi/2)}/\sqrt{2} + v\,Ee^{-i(\varphi 2-\varphi)}/\sqrt{2}. \end{aligned} \tag{5}$$

$$\begin{aligned} O_2 &= R_{I2+}T_{I1}, \\ &= v\,Ee^{-i(\varphi 2-\varphi-\Pi/2)}/\sqrt{2} + v\,Ee^{-i(\varphi 1-\varphi)}/\sqrt{2}. \end{aligned} \tag{6}$$

So the amplitudes of the transmitted and the reflected beams are $e^{i\varphi}/\sqrt{2}$ and $e^{i(\varphi+\Pi/2)}/\sqrt{2}$. Then there device's bandwidth occurrence was found at 0.188 to 0.188 GHz. The maximum absorption ratio obtained was 17 dB, and the highest extinction ratio achieved was 0.199a. Hou et al.[20] suggested a self-collimation (SC) waveguide that was polarization insensitive as seen in Fig. 3. The suggested design concentrated primarily on two parameters, namely, the interior rod with circumference r and the outer perimeter radius R, to move the SC band to a particular wavelength. R was positioned at $0.46a$ while radius was changed from $0a$ to $0.4a$ in the first scenario. The external ring radius R was modified from $0.26a$ to $1.49a$ in the instant occasion, with r set at $0a$. SC was moved toward that different frequency by reducing the interior rod radius r and reducing the outermost circle radius R, as shown in the result. This dissipation factor brightness system has a width of upto 102.9 nm.

Fan et al. proposed another all combinational logic construction for the PIC that included OR, XOR, AND, and NOT gates sort of self beams.[21] The structure was constructed by means of a 2D square lattice pattern using Si as the background materials. The holes have a dimension of $0.3a$, where the lattice constant a is the diffraction property, which is 0.4185 μm, and the electrical resistivity of the supplemental information is 11.56. Two line defects, A and B, were added in the orientation and training in Fig. 4; they functioned at a different frequency of 1550 nm and had double splitters S_1 and S_2 constructed by altering the rod size between 0 to $1.6a$. Their design was created mainly on the phase difference between the incoming signals, which is the phenomenon that occurs as self-collimated beam. When luminous feedback at the information connector A in comparison with port B was of equal intensity, the information beam out of A was partly

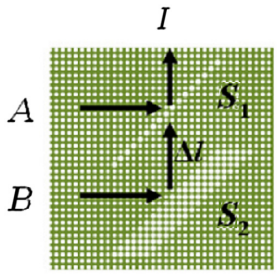

Fig. 4 NOT and AND gates, with Δl indicating the separation between two splitters and l indicating the output.[22]

absorbed where the beam from B was wholly reflected, but when this beam interfered, there was an output at the phases that was dependent on the different stages at the inputs and had constructive or destructive interference.

Self-collimated beam method as XNOR gate, NAND gate, AND gate and NOR gates were presented in Ref. 22. The structure was created utilizing triangle lattice architecture with Si rods position on an air environment. The chosen holes have a radius of 105 nm and a lattice parameter a of 302 nm. By dropping the radius of 15 rods in the x and y directions, two line deficiencies were generated, with a spacing of $10a$ separating them. After that, the defective diameter was modified, but it was discovered that when the fault rod length was around 83 nm, the receiving and reflection transmission lines was comparable.

When defect rod circumference was more than 83 nm in another scenario, a phase angle of $\Pi/2$ was attained connecting the power transmitted and the received power. Two indications of the input signals (I_1 and I_2) were supplied at fault 1 and a corresponding output (Iref) was sent at fault 2, as shown in Fig. 5. Both frequencies function at 1555.1 nm. The input signals and corresponding output were position to $2\,Io$ and $0.5\,Io$, correspondingly, for the proposed framework to act as an AND gate. It competes constructive or viciously at defect 2 dependent on the phase angle delivered at the intake with regard to the generated signal. As there were no signals at the intake, Iref ($0.6\,Io$) at fault 2 was evenly split; transmission were sufficient, its mirrored half interferes with defective 2, and the output level of $0.25\,Io$ was recorded at the out, which was regarded as "logic 0." "Logic 1" was defined as the concept larger than 0.25 Io.

The architecture in 2D PhC presents a self-collimated beam and the splitting phenomena.[23] The model was built out of Si ($n = 3.52$) rods arranged in a triangular diamond lattice in an air background. By adjusting the faulty hole width to $0.286a$ and the adjacent hole zone

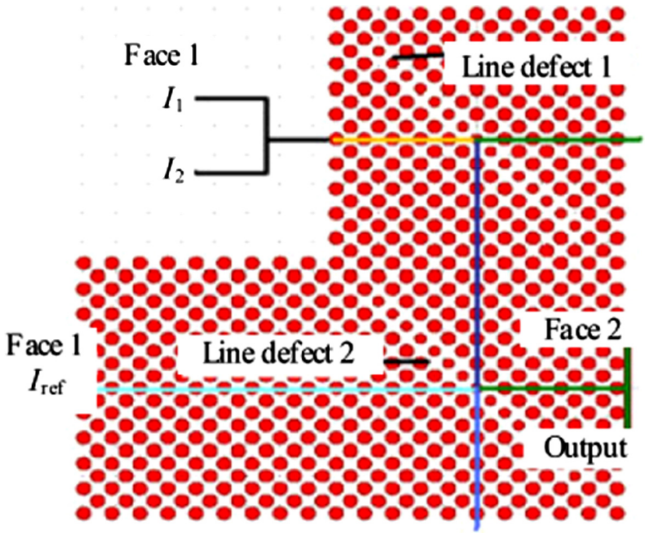

Fig. 5 Using a self-collimated light with dimension 20×21, a design of NAND, XNOR, AND, and NOR logic gates is shown Ref. 22.

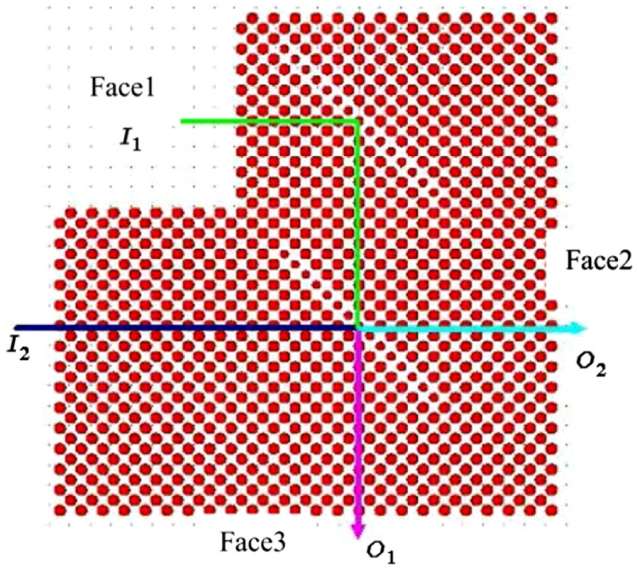

Fig. 6 Propose 24 × 25 XOR and OR gate.[23]

circumference to $0.35a$, two line defects were generated in the x direction in the basic techniques. The imperfection had a smaller radius because it caused a phase difference of $\Pi/2$ between transmissions and reflected rays. Figure 6 shows the two input ports I_1 and I_2 as well as the two voltages O_1 for the OR logic and $O2$ for the XOR logic.

Figure 6 where a phase difference of $\Pi/2$ was provided at I_1, it interfered affecting I_2 at the succeeding procession fault, resulting in absorption and scattering at O_1 and O_2.

For the use of photonic-integrated nanostructures, the AND gate self-collimated beam was presented in Ref. 24. In an air background, a lattice 2D PhC architecture with Si ($n = 4.46$) rods was employed. The breadth in the X-direction was $23\sqrt{2}a$, while the length in the Z path was $25\sqrt{2}a$. As shown in Fig. 7, the structure comprised of two line flaws with a flaw rod radius (r_d) of $0.275a$ (a 302 nm). The received and mirrored powers were evenly distributed when r_d was $0.275a$. The time margin connecting received and mirrored beam was 2 when r_d was more than $0.274a$; otherwise, it was 2. $I_1 = I_2 = I_o$ and the situation indicator signal, $I_{\text{ref}} = 0.6\,Io$ are used in the AND gate operations. Direct or indirect interaction occurred depend on the phase difference functional at various input ports. Interfering pattern served as the AND gate's output. When no inputs were provided, $0.5\,Io$ was split evenly between two yield ports, resulting in $0.26\,Io$. Once equal inputs are supplied, the outcome at defect 1 was $2Io$, but after traveling though

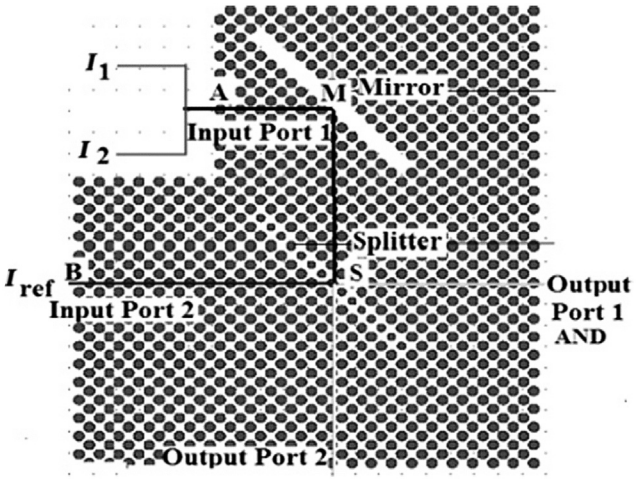

Fig. 7 Structure of AND gate 26 × 25.[24]

imperfection 2, where destructive interference occurred, the output became $0.75Io$. The $0.24Io$ thresholds were used to differentiate either logic 1 or logic 0. The suggested AND gate's average area was $25 \times 10\ \mu m^2$, and the entire response time was <2 ps.

5 Optical Logic Gates based on Bandgap

Many scholars offered different architectures for constructing various gates, as given in Table 1. Gates were mostly created and implemented with AND, NAND, XNOR, and XOR gates. Various researches proposed using a Si rod in an air background. However, in the instance of CR, Christina and Kabilan's construction for NOT had the greatest result, i.e., 30 dB. Additionally, gateways constructed with a self-collimated beam have a number of drawbacks, including a low CR, a huge area, a high price owing to the big size, and signal steering in the positive and negative directions. The upsides of non-bandgap gate and all-optical logic gates are their ease of configuration and reduced computational cost, while the disadvantages are their low CR, the need for power switches, the huge area procured and the large cost leading to large area.

The bandgap of the design is utilized to locate hidden radio frequencies that are unlikely to reach through material in bandgap-based all-optical gates. By adding various forms of faults, one of the suppressed harmonics is able to spread across the framework. Multi-mode interference (MMI), nonlinear Kerr impact, and electromagnetic interference are commonly used to create interruption logic gates. MMI configuration-based AND and NOR gates, as can be seen in Fig. 8(b), were introduced in Ref. 33, with B and A as inputs and O_1 and O_2 denoting fixed phase and amplitude. The self-collimated imaging phenomena are the idea that MMI devices operate on.

In the active region, there were guided oscillations, which indicated interfering. Although in MMI, input parameters are often indicated by the two inputs phase and amplitude, and binary phase shift keying (BPSK) signals are employed as input variables. In other respects, depending on how the multiple input stage data interacts with MMI, either a message is generated at the input, which was regarded as logic 1, or a pattern was degraded, which was regarded as logic 0. The MMI structure is known as a transceiver, sending the outputs to the one of the output pins. This is accomplished by building the MMI coupler with the right choice of attributes for the phase angle to acquire output from the specified port. The threads in the suggested structure were made of Si, while the background was air arranged in a squared lattice pattern. The XOR/XNOR configuration has A and B as input and X and Y as output port, as shown in Fig. 8(a). There was a small variation of phase at ports A, logic "0" was represented as input signal with phase shift Π at port A, while logic "1" was declared with m stage either at port B, gate "0" was represented with a phase angle of $3\Pi/2$, while logically "1" in phase $\Pi/2$. To realize the AND gate shown in Fig. 8(b), phase 0 signified reasoning "1," and port A and B combined phase 0 constituted logic "1." With a phase shift of $\Pi/2$, logic "0" were established at O_1 and O_2. The main change in the NOR gate that O_1 and O_2 are at logic "1," which was denoted by a phase shift of $\Pi/2$. The AND operation had a CR of 21 dB and also the NOR action had a CR of 19 dB.

AND and XOR logic approach on MMI were planned, as shown in Fig. 9, where A and B input pin X and Y output ports.[34] It was made with Si rods and triangular mesh geometry with SiO_2 as the background component. The structure's lattice constant is r, and the rods at the bends have radius rw, rx, ry, and rz, which were chosen for maximal propagation at the output pins. The width W of $2\sqrt{3}$a and the lengths L were selected for the MMI area, where Wn denotes a bandpass filter constructed by completely eliminating n lines of rods in PhC. The amount of time it took to create the XOR gate was resolute by the length of time it takes to build the XOR gate. An input data with a phase angle of was given at port A, articulate logic "0," while a transmission with a phase angle of was started at port B, communicate logic "1," thus generating logic "1" at the inverter output. There was a production of logic "1" at the productivity since there was a stage of at terminal A, which indicated logic "0," and also an additional message with stage shift 2 at port B, which represented logic "0." In another situation, logic "0" was identified at the input when a transmission with an amplitude and phase of at the effort source A stated logic "0" where the message through the stage two at port B declared logic "0." The output port sensed logic "0" when all effort at plug A and plug B matched "1" with stage shifts of 1 and 2. By varying the length of MMI to 10a and appropriately choosing op amp phases, the AND gate was created using the same construction. For both AND and XOR, a CR of roughly 6.79 dB was attained.

Table 1 Shows a comparison of several categories of all-optical gates based on non-band gap.

Ref. No.	Lattice type	TE/TM	Gate	Area	CR (dB)	Baud rate (Tbit/s)	Operating wavelength (λ)	Lattice constant (a)	Rod material	Background material
25	Square (rod in air)	TE	OR gate, XOR gate	—	18	—	$1/0.185a$	—	Si material	Air
26	Square (air holes in Si)	TE and TM	Waveguide for gates	—	—	—	1551 nm	420.05 nm	Air	Si
27	Square (rod in Si)	TE	NOT gate, OR gate, AND gate, XOR gate	—	31	—	1561 nm	0.4186 nm	Air	Si
28	Square (rod in air)	TE	NOR gate, NAND gate, AND gate, and XNOR gate,	—	7	—	1555.2 nm	302 nm	Si material	Air
29	Triangle (rod in air)	—	XOR gate, OR gate	—	—	—	1551 nm	366 nm	Si material	Air
30	Triangle (rod in air)	—	AND gate	25×10 μm^2	—	—	1.5 μm	0.45 μm	Si material	Air
31	Triangle (rod in air)	—	AND gate	110 μm^2	—	—	1.5 μm	125 nm	Chalcogenide	Air
32	Square (rod in Si)	—	NOR gate	68 μm^2	—	—	1.55 μm	0.56 μm	Si material	Air

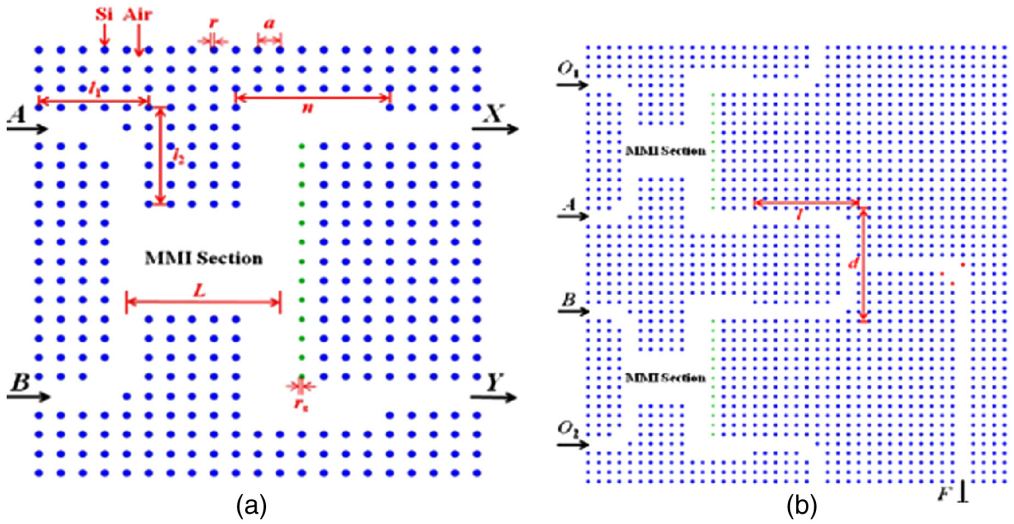

Fig. 8 (a) construction of 21×23 XOR/XNOR gates and (b) construction of 41×50 AND/NOR gates.[33]

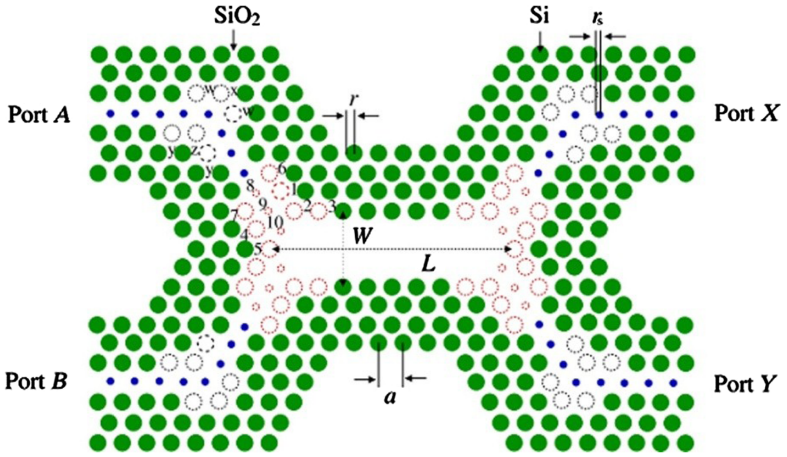

Fig. 9 Representation of 28×11 XOR gate and AND gates approach in MMI.[34]

Another MMI-based on the construction for all gates, as shown in Fig. 10, was presented in Ref. 35, with A and B as input port and C and D as productivity output side. The structure was designed using a hexagonal lattice topology of PhC with Si filaments as the background materials, with a crystallite size a and diameter of r. Rod B has a circle of R, and rod A was optimized with the MMI area of widths $W5$ and length L is taken as $4a$ by dividing the distance d of $0.5a$. In the XOR, logic "1" was defined by an input having stage 0 for input port A, whereas logic "0" was addressed by a message with a phase angle change of Π conveyed logic "1" for port B. Every one of the valves was created by combining the phases of the incoming signal at input port A and port B. In the C-band, the attenuation ratios for the AND, XOR, OR, and XNOR valves were 28.7, 28.7, 26, and 26.7 dB, respectively.

Using the notion of BPSK communications in MMI, the XOR, XNOR, and AND gating were devised. The apparatus was built with Si ($n = 3.4$) rods agreed in a lattice structure in an air background. The radius width was position at 0.18a, where the structural parameter, which had a frequency of 522 nm. The structure's operational frequency was 0.334 to 0.342 (a), approximately corresponded to the C-band. The XOR/XNOR gate has two parameters A and B, as well as slightly different X and Y, as shown in Fig. 11(a). To ensure higher power at the outputs, extent l_1, l_2, and L were altered and originate to be $6a$ and $8a$, correspondingly. Phase Π represented logic 0 on entry port A, while phase 0 signified logic 1 on another input port B.

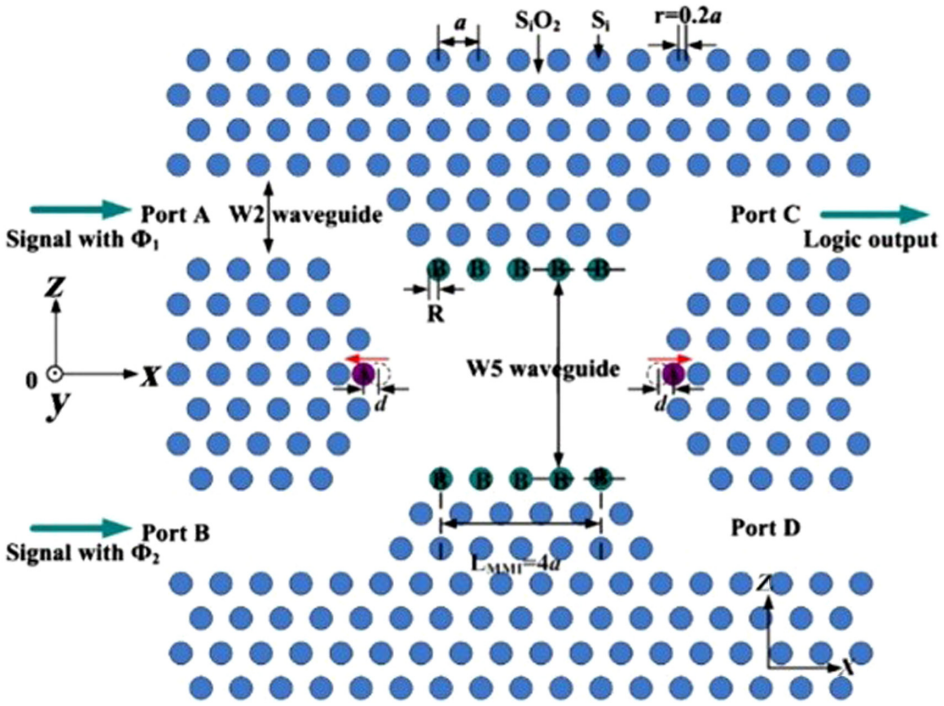

Fig. 10 Using hexagonal matrix structure 17 × 10 NAND, XNOR, XOR, and OR logic are shown schematically.[35]

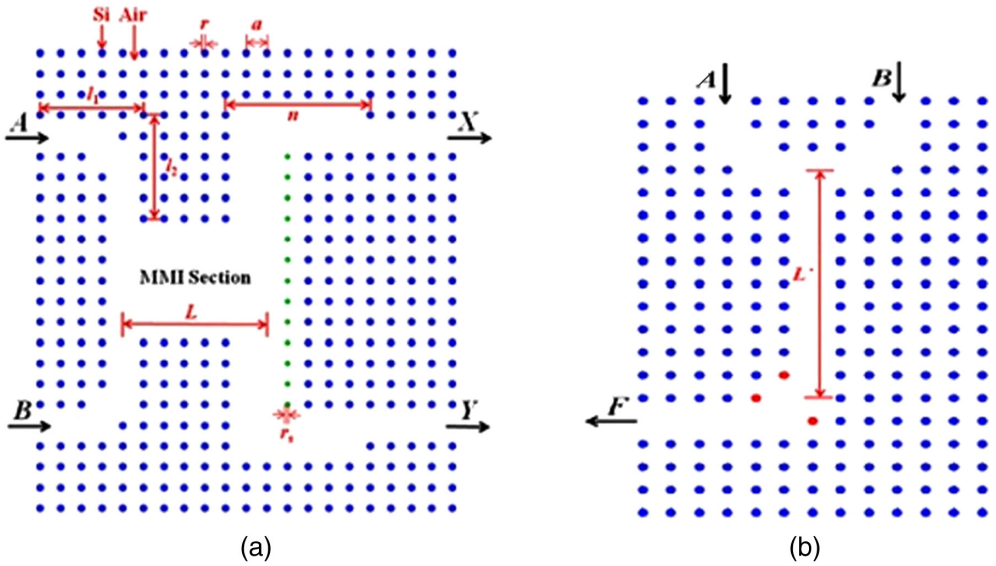

Fig. 11 (a) Sketch of 21 × 23 XNOR/XOR using BPSK indication and (b) configuration of 13 × 19 AND gate with nonlinear Kerr substance rod.[33]

Phase $3\Pi/2$ represented logic 0 while phase $\Pi/2$ denoted logic 1. XOR and XNOR gates were created using this phase arrangement.

Another AND gate construction was developed, consisting of an $L-b$ interferometer, as seen in Fig. 11(b). As shown in red in Fig. 12, present be thrice Kerr nonlinear types shafts with a permittivity of 7 and a radii of $0.19a$. There were two data ports A and B, as well as one sending end F, in the construction.

To ensure higher wattage at the outputs, lengths l_1, l_2, and L were altered and discovered to be $6a$ and $8a$, accordingly. Phase Π represented logic 0 on entry port A, while phase 0 signified

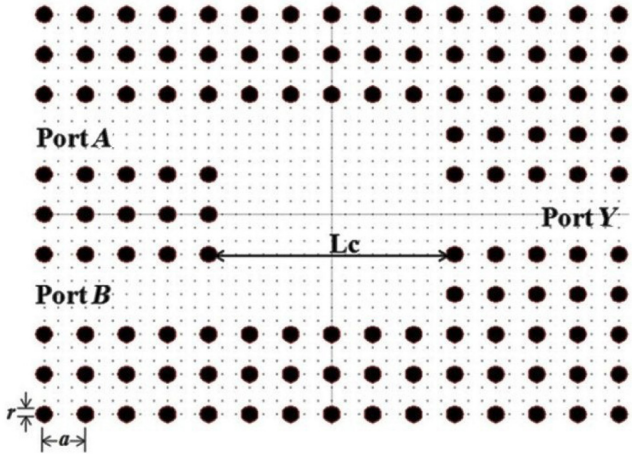

Fig. 12 Impedance matching entanglement design for 15×11 OR, XNOR, XOR, and NAND gates.[36]

logic 1 on another input port B. Phase $3\Pi/2$ represented logic 0 while phase $\Pi/2$ denoted logic 1. XOR and XNOR barriers were created using this stage arrangement.

Another one gate construction was developed, consisting of an L-branch interferometer, as seen in Fig. 11(b). As shown in red in Fig. 12, there were three Kerr regressive types shafts with a permittivity of 7 and a radius of $0.18a$. There were two data ports A and B, as well as one sending end F, in the construction.

As shown in Fig. 12, the structure had input data ports A and B, as well as a production port Y, with a radius of $0.2a$. To create two fold pictures of the input, the coupler duration of $6a$ was chosen correspondingly. The input values were expressed as phases, whereas the return was expressed as intensity. At the outputs, direct or indirect interference happened depending on the timing used. Caused by a single fold of maximum concentration, a lead up was detected at the productivity port Y when the stage angle in between two inputs was 0. Two input streams never overlapped with one another and were reflected back to the initial line when the phase shift was Π. When phase angle was $n2$, the lights from the port 1 were overlaid, and the strength at the output side Y was much the same. NAND, XOR, OR, and XNOR circuits were realized using separation arrangements. At wavelengths of 1551 nm or a fast retort of 0.131 ps, the CR for XNOR/XOR logic was 40.41 and 37.40 dB for OR/NAND electronics.

The AND gate construction, which is approach on asymmetric Kerr materials, was described in Ref. 37. Kerr systems has the potential to change the molecule's optical properties simply altering the input.

The dielectric properties were computed using the formula $n = n0 + nI$, in which I denoted the concentration, $n0$ the linearly refraction directory, and n the Kerr exponent. The dielectric constant altered as the strength of the original signal increased or decreased, changing numerous features of the construction, such as frequency band, etc. As shown in Fig. 13, the device several of two non-linear ring resonators, one of which works as an add-drop resonance. The device was built using PhC. with GaAs rods and a background material of borosilicate, which has observed refractive index of 3.59 and 1.507. Si nanocrystals, with a refraction difference of 3.40 and a Kerr coefficient of 10^{-16} m^2/W, were employed to construct the resonators. In the TM mode, the signals were polarized. For regressive substance with a resonant frequency of 1550.9 nm to function as the operational wavelengths for the AND gate, a resonance built of manifold structure was needed, as illustrated in Fig. 13, with a drop resonant frequency of 1548.4 nm and effort influence of 33 Wm. The ports were named A and B, with port P linked to the message function, as shown in Fig. 13. There was a transmission at either A or B, the information from P linked with the top resonant cavity, allowing no information at P.

When the data was delivered at port A, it linked with the top resonant cavity, but signal P was unable to interface with the top resonant cavity owing to a shift in the echoing frequencies, therefore signal P attached with the other lower resonant cavity, preventing any signal from reaching the output port. The indicators at both ports A and B are connected with the superior

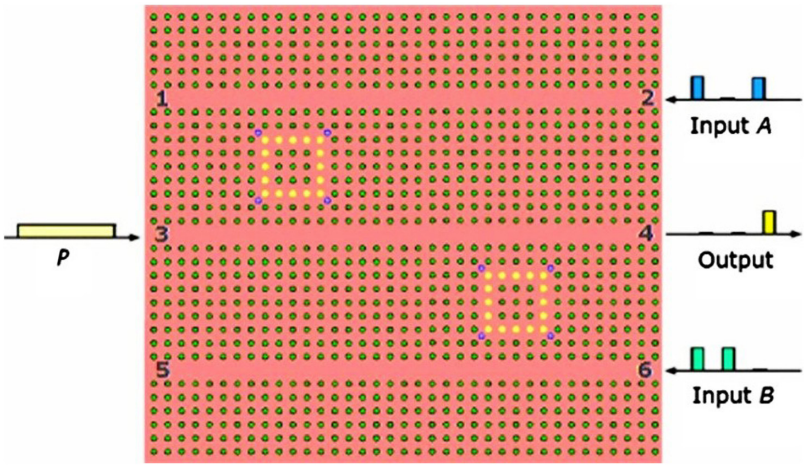

Fig. 13 AND gate diagram of 37×33 nonlinear Kerr substance.[37]

and inferior resonating cavity; however, indicator P had no method of coupling, resulting in logic "1" being recorded at the inverter output. The suggested logic gate has a bit rate of around 120 Gbits/s.

Pashamehr et al.[38] presented other configuration for NOT/AND/OR gates due to the nonlinear Kerr material. As shown in Fig. 14, the structure contains inputting ports *C* and *D*, a baseline port linked to the message function, and an output terminal *B*. The ring resonant in the heart of the structure, which repeats at a particular frequency, was created using asymmetrical Kerr semiconductors. The signals from *A* connected with the resonant cavity and there was no intake at ports *C* or *D*, and that there was no exit at input Ports, which indicated logically "0." When stage *C* or *D* acquired output, they were connected with the resonant cavity, or the operating frequency altered, causing the signals from port *A* to spread to stage *B*, which signified logic "1."

As shown in Fig. 15, a construction for the NAND gate was presented in Ref. 39, which combined the notion of nonlinearity in Kerr material with a PhC approach resonant cavity. The ring reverberation of the original scheme was created using a 32 square arrangement of chalcogenide rod ($n = 3.1$) in air. The radii were chosen to be $0.2a$, with the being the lattice parameter of 640 nm. The PBG for the geometry was computed, and the optimum wavelengths were determined to be 1554 nm.

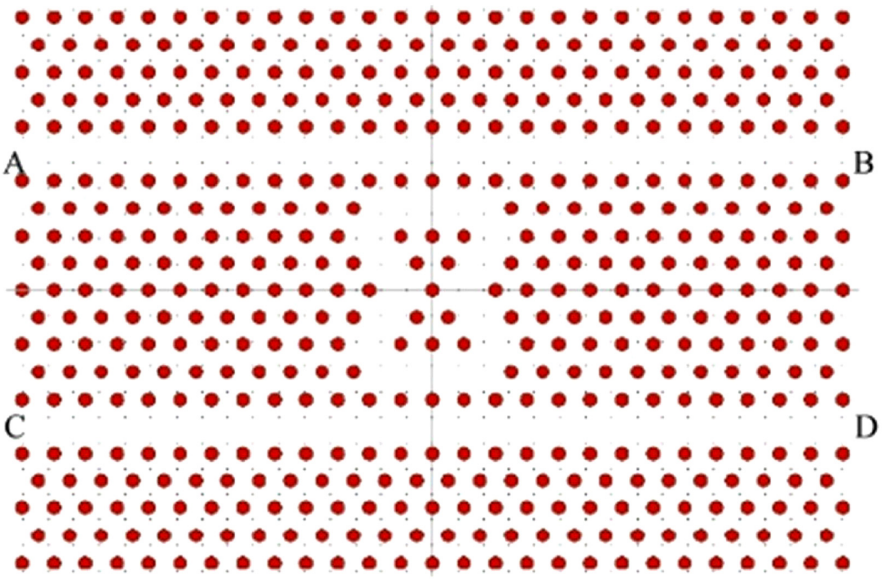

Fig. 14 27×10 OR gate diagram employing asymmetric Kerr substance.[38]

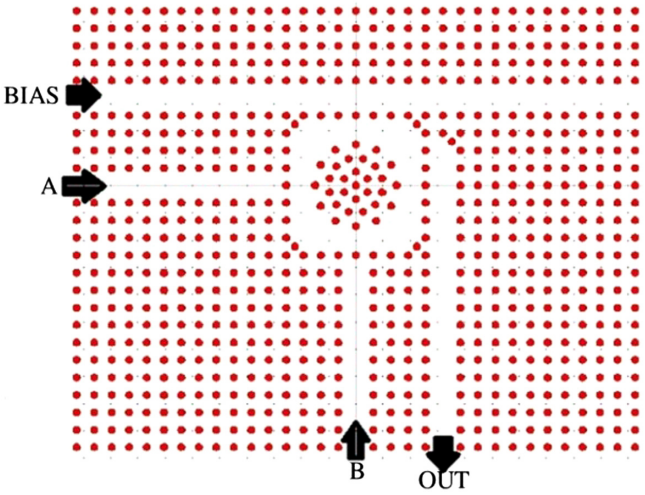

Fig. 15 33×26 irregular Kerr configuration of a NAND gate.[39]

After developing the resonators, it was discovered that at a power density of 0.5 $\mathrm{KW}/\mu\mathrm{m}^2$ or larger, the molecule's refractive index shifted owing to the Absorption coefficient, changing the ring's resonating wavelengths make your way to the inverter output. The NAND gate construction was constructed utilizing 33×26 rectangular diffraction gratings of insulating rods after the ring resonant was developed. As observed in Fig. 15, it had three inputs: *A*, *B*, and BIAS, as well as an output terminal called OUT. The oscillation frequency echoed in the rings and the result was created at the OUT stage; alternatively, there was really no productivity, proving the variation in logic of the NAND gate.

The construction of the NOT and AND gates approach on nonlinear Kerr material, as can be seen in Figs. 16(a) and 16(b), were suggested in Ref. 40. The construction includes a split ring that links to the input and output waveguides. With chalcogenide glassy rods and an air backdrop, a square lattice PhC geometry framework was employed. With TM polarized transmissions, the dielectric constant and Kerr factor of chalcogenide glass were 3.1 and 9^{-17} m^2/W, respectively. The ringed resonator's drop frequency wavelengths was 1550 nm, causing the energy content to exceed 1 $\mathrm{KW}/\mu\mathrm{m}^2$, which is the recognized lower limit. The operational wavelengths of 1550 nm was used in AND activities, as shown in Fig. 16(b).

Only the information after interfacing within the resonant proceeded to stage *O* in Fig. 16(a), which symbolized the NOT gate, since there were inputs at port a, and no indicator existed the outlet *O* in Figs. 16(a) and 16(b). When a message was provided at both input pin A and B in that One and gateway construction, the intake at B being linked with the resonant, while the output via port *A* was transmitted to port *O*, which signified the logical "1."

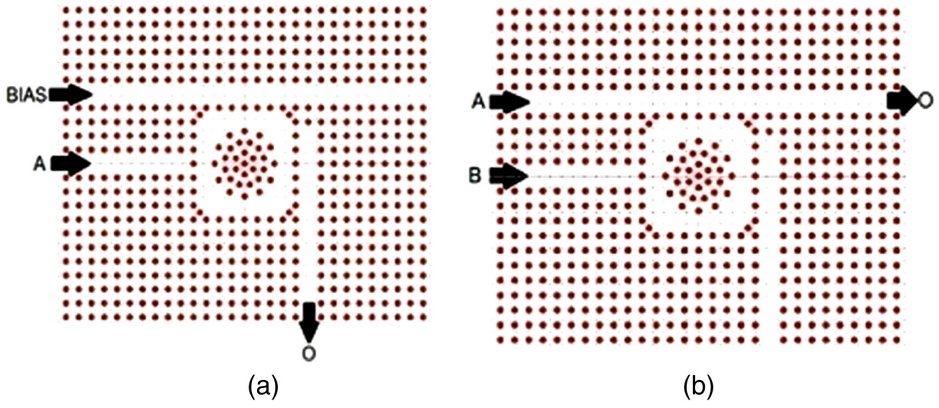

Fig. 16 (a) 29×23 layout of NOT gate and (b) 29×23 layout of AND gate.[39]

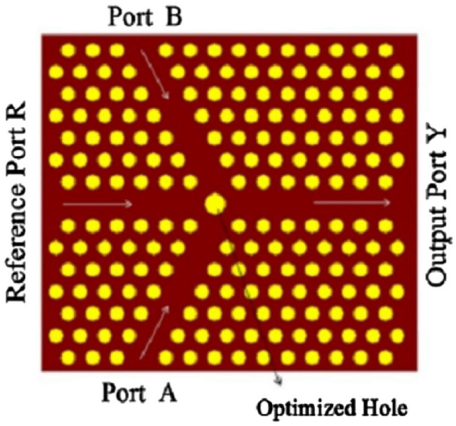

Fig. 17 Representation of 15×7 XOR, NAND, NOT, OR, AND, NOR, and XNOR.[41]

On the concept of interruption in the PhC, OR, NAND, NOR, XOR, NOT, AND, and XNOR gateways were presented in Ref. 41, wherever *B* and *A* were the input stages and stage *R* was the reference stage, again was modified appropriately to operate as a particular logic, as shown in Fig. 17. The kind of defect generated throughout all logic gates with resonance faults varies.

The circuit uses the occurrence of interference to rebalance the gate's outputs. Adjusting the period of the input allows the interference defect based all-optical and gate to be created depending on whether constructive and destructive interference occurs at the output. Logic "1" was represented by diffraction grating, whereas logic "0" was given by constructive interference. The structure was built with Si rods and air as the background element on a rectangular matrix PhC shape. By eliminating the holes, rectangular diffraction gratings were produced, and the hole in the middle was tailored to maximize reception at the inverter output. The operational signals were polarized using the TE method. There is no indication at the *A* or *B* stage and the *R* indication were position to a phase shift, logic "0" was created at the yield pin to realize the AND gate. If either input was position to input Port with the phase difference of Π or the feedback controller was positioned high with a phase angle of Π, destructive interfering was formed and logic "0" was seen at the ports from *A* to *B*. There was high frequency and logic "1" was formed at the inverter output if the values for both outputs were given and also the indicator R. OR, XOR, NOR, NOT, NAND, and XNOR are logic procedures.

A configuration for executing AND, XOR, OR, and XNOR gates is predicated on the influence effects with *A* and *B* as inputs and *R* as reference point,[42] as shown in Fig. 18. The architecture with small gaps and Si as the background materials was designed using PhCs

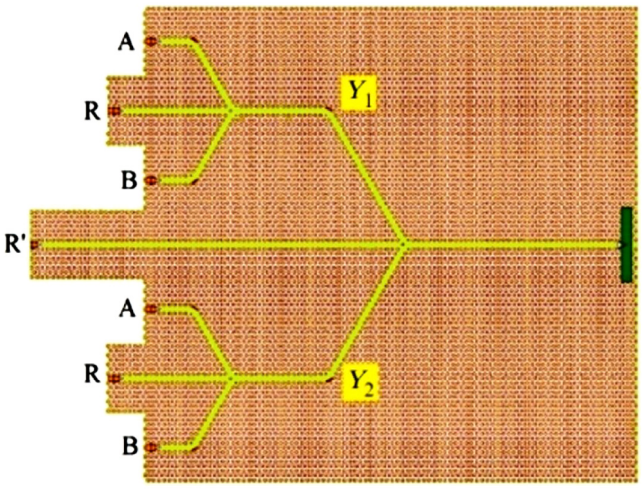

Fig. 18 Layout of AND gate build with NAND gate.[42]

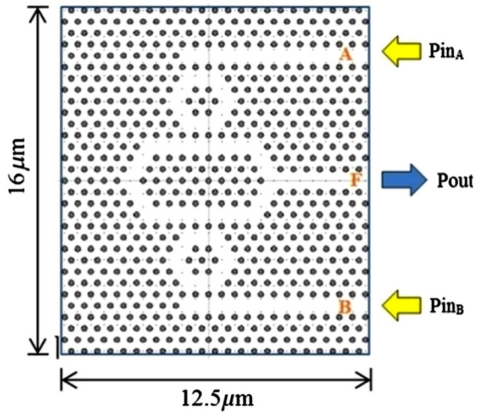

Fig. 19 Construction of 23×15 OR gate with A and B as input.[43]

triangular honeycomb topology. All of the gates were achieved using the perfect mixture of NAND, and the input signals were TE polarized. To realize AND gate, the baseline stage of the outputs A and B were situated to 0 in all permutations with the message R with phase. $R = 0$ had the opposite phase of the signal R. Several gates use the same principle of various combinations. A construction for the OR gateway based on the MZI was presented in Ref. 43. The rods were made of Si, using air as the background medium, and the structure was formed on hexagonal network geometry. As shown in Fig. 19, the MZI is at the heart of the construction, with superior and inferior add-drop resonators coupled to the two port arms port A and port B. The operational frequencies were polarized in the TE direction. To produce the interference patterns necessary to actualize the OR gate, the MZIs two arms are of identical height.

There was an emission recognized at the output stage indicating logic "1" and with the indication at it from both source sides if one of the inputs was propelled among Port A and Port B; it interfered productively owing to having an identical height on MZI arms, and signified logic "1. "

D'souza and Mathew presented another construction based on the interaction effects for implementing OR, XOR, NAND, and NOT gates have inputs designated A and B and an output pin named O.[44] The system was designed using square lattice structure, utilizing Si substance again for rod with gas as the medium.

There had been a ring resonance and beam splitters produced by disconnecting the shafts that were coupled to the source and load, as shown in Fig. 20. The two inputs are polarized in the TM direction. There was a linkage of two inputs in the oscillator whenever a wave was present at either A or B, with one component propagating in a clockwise manner (CW) and the extra in a counter-clockwise manner (CCW). At the input of the outgoing waveguide, both the CW and the CCW interfered positively, resulting in logic "1"; once both frequencies were delivered owing to symmetrical, they reacted constructively, resulting in logic "1" at the outputs. Different gates were constructed by optimizing the dimensions of the resonant cavity, including entire width.

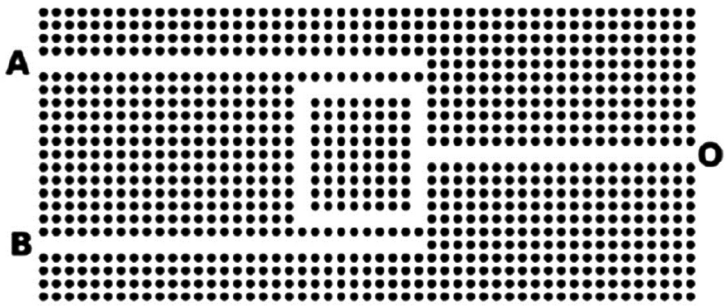

Fig. 20 Construction of 55×23 OR gate with A and B as input.[44]

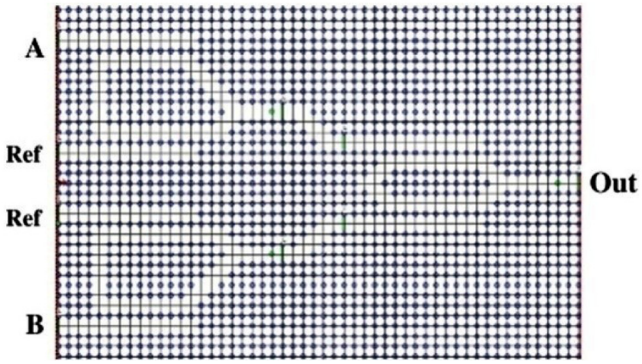

Fig. 21 Structure 52×35 for NAND gate.[45]

In Ref. 45, a framework for implementing the NAND gate was presented, as well as alternative architectures for realizing all logic gates. The building was constructed approach this lattice topology with semiconductor rods on an air black background. All of the output and ref messages would be in synchronization for the realization of gating. The XOR gate was represented by 1 in Fig. 21, whereas the OR gate was denoted by 2. The NAND gate was created by combining OR and XOR barriers in a unique manner as shown in Fig. 22. Each XOR gate's one inputs and a corresponding output were both position to logic "1," resulting in the result of every XOR gate being the counterpart of its incoming signal. Two diffraction gratings were created to connect the XOR gates' output to the OR gates while keeping the transmissions in phase. The ref indication created logic "1" at the XOR outputs since there were no impulses at input A or B, and when it got the OR device, it created gate "1" as output. When present was contemporaneous input at A and B, constructive interference occurred, resulting in logic "1" as the outputs of one NAND gate and "0" as the result of someone else, which when amplified via the OR gate yielded logic "1."

A square lattice architecture of Si rod in an air background like another construction for NAND and NOR switches based upon that interference phenomena.[46] The outputs of the AND/OR digital circuit was inverted using the NOT gate at the outlet as shown in Fig. 23. The rationale was flipped by the NOT gate due to the phase of the REF2.

REF2 barred the AND/OR logic gate's outputs if it was logic "1" owing to stimulated emission with the AND/OR logical gate's conclusion. Since the phases of 1 had no effect when phase 2 delivered gate "1" at the output Sequence, there would be little power transferred owing to constructive interference if the AND/OR logic result had logic "0." All alternatives were accomplished that use these various phase ratios. OR, XOR, NOT, The OR gate logic was accomplished when

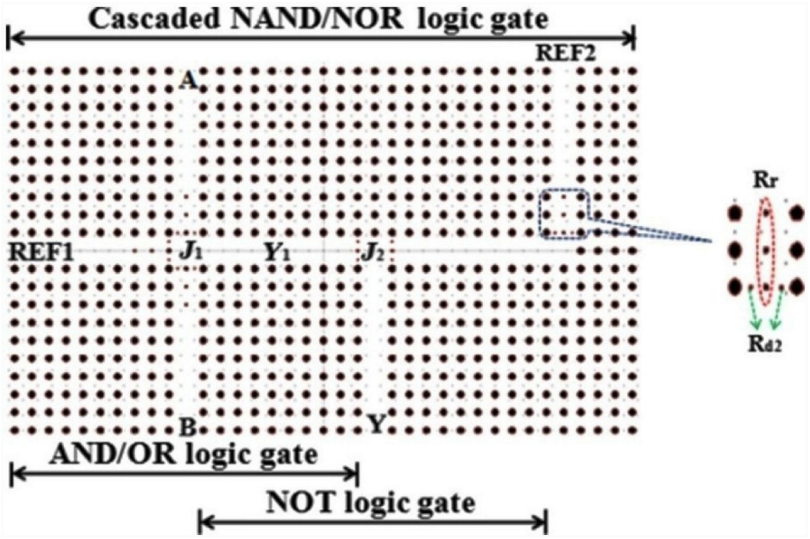

Fig. 22 Flow logic gate for 38×21 NOR/NAND functions.[46]

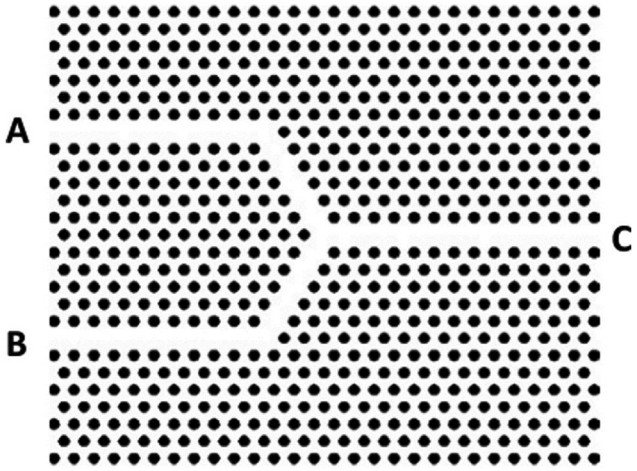

Fig. 23 Configuration for 28 × 14 OR gate in 2D PhC.[47]

light went via output device *C*. The line imperfection for inputs *B* was enlarged for the XOR gate to prevent constructive and destructive interference, and other such crossings were created by altering the height of line gap and introducing reference current. The suggested design attained the greatest CR of 20 dB. Two distinct AND, OR logic gate architectures were presented in Ref. 48. The dielectric constant, radius, and crystallite size, all of which were 3.59, 0.2 m, and 0.54, respectively, were unchanged in both configurations. Both nanostructures were organized in a hexagonal honeycomb on a background of the round Si rods. The and gate has two data defects, two sphere gaps, and one *Y*-branch tunnel, as shown in Fig. 24(a). *A* and *B* were used as outputs.

Y was the outcome, whereas *X* was the input. The input wavelengths were tuned to 1.5 m, which corresponded to the ring cavity centre wavelength. The output became logic 1 if data was present at any or perhaps both ports; alternatively, this was logic 0. There had been line faults, four ring cavity, and one *Y*-branch wave front in the AND circuit, as shown in Fig. 24(b). Two ring chambers were introduced though they can decrease the frequency further, resulting in reduced signals reaching the outputs. The output with an amplitude of <0.5 was judged logic 0, confirming the AND portal's reasoning, but the OR gate's signal strength was more than 0.5. The quoted data rate for the OR and gates presented a new construction for XNOR, NOT, NOR, and NAND gates approach on the interfering issue.[49] Si rods were placed in an insisted shape in the air. Two constructions were suggested, one in the NOT gate that used one T-waveguide and another for the XNOR, NAND, and NOR circuits that used Both *T* waveguides produced by deleting holes. To conduct various logic operations, a references port with a 180-deg amplitude and phase was introduced. There was change in the direction when the phase difference was $2k\Pi$ and interference occurred. To decrease back reflection, tiny holes of crystal glass with refractive index 1.92 were introduced.

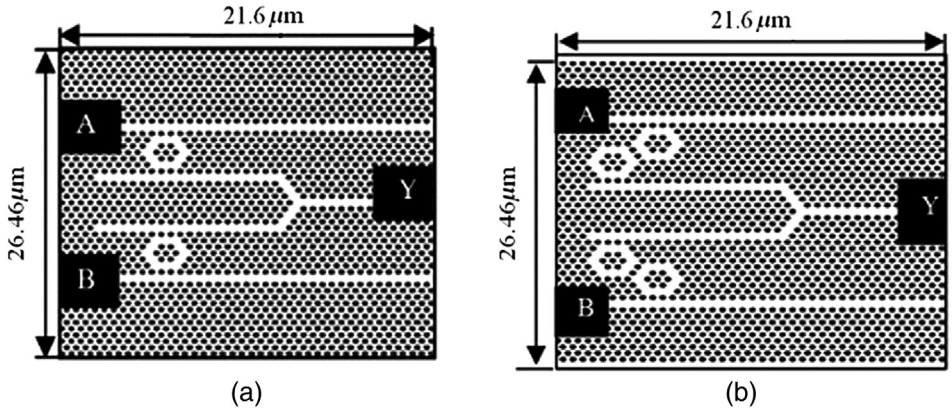

Fig. 24 (a) Configuration for 40 × 24 OR logic and (b) configuration for 40 × 25 AND logic.[48]

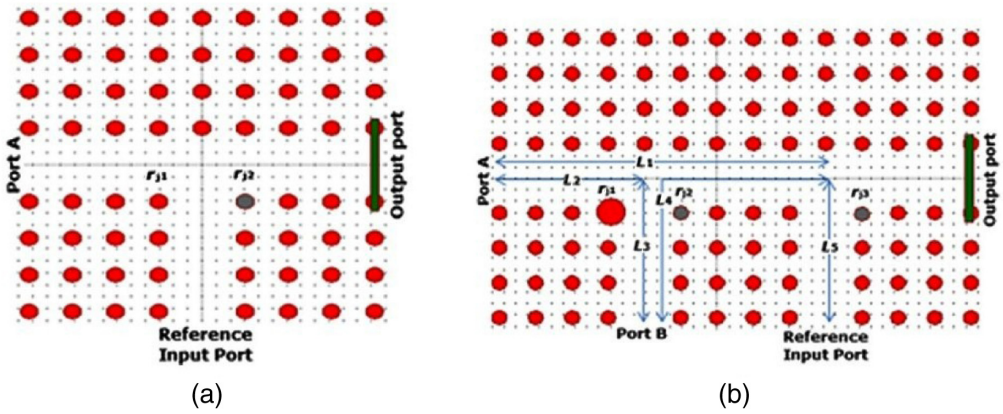

Fig. 25 (a) Configuration for 9×9 NOT gate and (b) configuration for 14×9 NAND and NOT gates.[49]

When port A and the other port inputs have been in phase, logic 0 was recognized in the NOT gate organization, as shown in Fig. 25(a), whereas logic 1 was discovered in other circumstances. The NAND, XNOR, and NOR gate structures in Fig. 25(b) were created by combining distinct stages of control signal. The suggested structure's quickest reaction time was 0.35 ps. The NOT was 5.04×5.04 μm^2 in size, whereas the NAND, XNOR, and NOR gates were 8.04×5.04 μm^2 in size.

A configuration for NOR and AND processing elements was presented in Ref. 50. The design will be based on the trapezoidal honeycomb architect of Si rods in velocity with just a network parameter.

The wavelength is 580 nm, and the rod radius is $0.2a$. Both gates were built using the same framework. It includes three inputs, A, B, and CTRL, as well as productivity, as shown in Fig. 26. Only in the instance of the NOR gate was the CTRL input made active. Three shafts with a radius of $0.6a$ were just not eliminated, as shown by the construction, to decrease back reflection. In the instance of the XOR gate, the outputs were the CTRL message if there had been no input, and there was no input in many other circumstances owing to two beams. The obtained bit rate for such NOR and AND gates was 1.54 Tbits/s.[51] Suggested the construction in Fig. 27 to execute all-optical AND/OR gates. With the Si rods in the air background, the arrangement exhibited square lattice shape. It was made up of one loop antenna that was optimized by adjusting the rod radius until it echoed at the occurrence response, and four waveguides that was created by detaching the rods and connecting to input ports A and B, as well as outlets 1 and 2. It had a $0.15a$ internal ring radius and a $0.2a$ rod radii, with a being the lattice characteristic. So that the feedback is terminal A but none input at port B, the signal beginning is connected as the reflector to their output in a CW happened in their outputs.

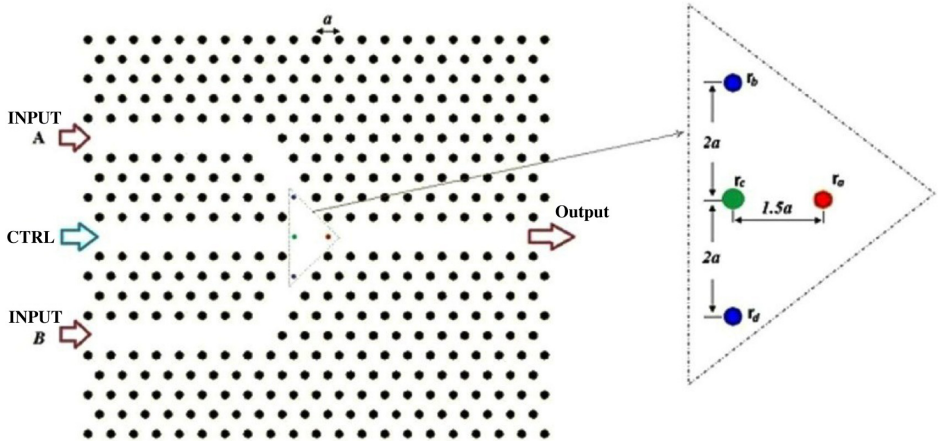

Fig. 26 Construction of 21×11 for NOR and AND gates.[50]

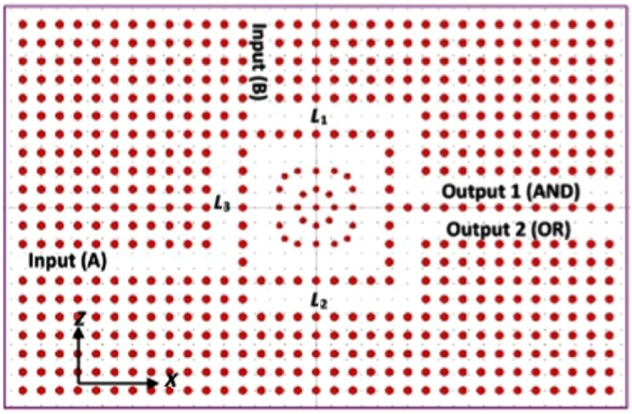

Fig. 27 Diagram of 33×21 OR/AND logic gates.[51]

There was no production at either inverter output even though neither input port had any input. That whenever A 0 and B 1 were used, the OR circuit was realized because the inputs from B got connected with the resonant cavity and had gate "1" at the output 2, but AND was achieved since the output port 1 was "0." There was high frequency while there were outputs at both inputs, resulting in "1" at two outputs.

Sankar Rao et al. developed another framework for creating NOR, NAND, and XNOR gates depending on the PhCs interference phenomena. Different logic gates were created by simply adjusting the phase of incoming signal.[52] The system was designed using square lattice topology in the air using Si material 0.6 m as shown in Fig. 28. It had two contribution plug A and B, as well as a referencing channel R, and several values were implemented. To achieve the needed output, various adjustments were made to specific rods in the construction. To attain the required output in the suggested structure, various reflection rods with varying radii were included for the reflected operation, namely, $r1$ 0.12 m and $r2$ 0.084 m. In the NAND logic, 1 correspond to a stage transfer of 0 degrees in the number of inputs "10" and "01," whereas logic 11 was portrayed by an amplitude and phase of 0 and 180 deg in the case of "'11." The phase of the reference signal was adjusted to 180 deg in "01" to produce useful interfering, and 180 deg in "11" to achieve interference. XOR and XNOR logic gates had the same layout. The main distinction was that these gates were accomplished by adjusting phase shifts amongst outputs. The bridge's operational range was 1550 nm. NOR, NAND, and XNOR logic gates obtained CRs of 17.59, 14.3, and 10.52 dB, correspondingly. The construction was 7.2×5.4 μm^2 in size.

Table 2 compares of interruption discovery all-optical logic circuits on performance criteria such as the CR and bit rate. For AND and OR gates, the system as part by Parandin and

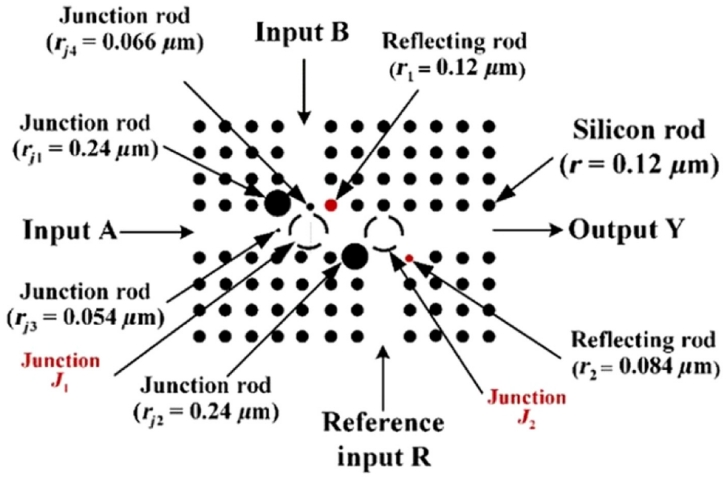

Fig. 28 Representation of 12×9 OR/AND logic gates.[53]

Table 2 Types of bandgap based all optical logic gates are compared.

Ref. No.	Lattice type	TE/TM	Gate	Area	CR (dB)	Baud rate	Operating wavelength (λ)	Network constant (a)	Rod material	Background material
33	Square (rod in air)	TM	XOR gate, XNOR gate, AND gate, NOR gate	—	AND-39 NOR-49	—	1530–1565 nm	532 nano material	Si material	Air
34	Triangle (rods in SiO_2)	—	NXOR gate, NAND gate	$9.90 \times 10.8\ \mu m^2$	XOR-13.3 AND-6.77	—	1550 nm	0.46 nano	Si material	SiO2 material
35	Triangle (rod in SiO_2)	TM	XXOR gate, OR gate, AND gate, NOR gate	$6.9 \times 6.7\ \mu m^2$	XOR-28.9 XNOR-28.7 NAND-28 OR-26.7	—	1531 to 1566 nm	432 nm	Si material	SiO2 material
36	Square (rod in air)	TE	XOR gate, XNOR gate, OR gate, AND gate	6.4×8.8 m	37.4–40.41	7.69 Tb/s	1551 nm	601 nm	Si material	Air
37	Square (rods in borosilicate crown)	TM	NAND gate	—	6.83	0.15 Tb/s	1550.8 nm	465 nm	GaAs material	Borosilicate
38	Triangle (rod in air)	TM	NAND gate, NOR gate, OR gate	—	—	—	1551 nm	726 nm	Chalcogenide glass	Air
39	Square (rods in air)	TM	AND gate	—	—	—	1555 nm	680 nm	Chalcogenide glass	Air
40	Square (rods in air)	TM	NOT gate, AND gate, NAND gate	—	—	—	1550 nm	630 nm	Chalcogenide glass	Air
41	Triangle (holes in Si)	TE	AND gate, OR gate, XOR gate, NOT gate, NAND gate, NOR gate	—	AND-8.76 XOR-8.49 NOT-5.42 NAND-9.59 NOR-5.42 XNOR-5.42	0.976 Tb/s	1550 nm	0.352 μm	Air	Si material
42	Triangle (holes in Si)	TE	NOT gate, AND gate, OR gate, XOR gate, XNOR gate, NAND gate	—	NOT-3.74 AND-11.47 OR-12.48 XOR-6.50 XNOR-6.50	0.461 Tb/s	1550	0.352 μm	Air	Si material

Table 3 Outline of the superior, fault, and possible application for each PhC logic gates move toward.

Logic gate method	Advantages	Weakness	Possible applications
SC Refs. 19 and 54	Small area faster response wide operating frequency bandwidth low power consumption	Low CR hard micro fabrication input phase requirement	Hybrid system integration Signal processing Extreme environments sensorsfrequency shifters
MMI Refs. 34 and 55	Small size faster response and large operating frequency bandwidth; low power consumption	Different phase for logic representation Input phase requirement	Splitters; demultiplexers Signal processing *E* tree environments sensors frequency; and shifter
Waveguide interference paths Refs. 25, 44, 47, 56–58	Wide operating frequency bandwidth low power consumption; fast response; and reasonable CR	Large size; difficult to synchronize the phase difference	Signal processing routing; parallel computing and hybrid system integration sensors
Nonlinear effects Refs. 26–30, 59, 60, 61	High CR input phase independent	Narrow operating frequency bandwidth high power consumption; and slow response	Signal processing switching; integrated photonics devices; and logic circuits

Karkhanehchi has the greatest CR of 18.96 dB and a baud rate of 6.77 Tbits. The gating approach mostly on electromagnetic observable fact have a higher CR and are easier to construct than gates relying on other occurrences.

6 Photonic Crystal Logic Gates

This section gives an overview of the numerous methods for performing logic devices in fiber lasers. For every gate, the phase of the two inputs is all that is needed to calculate its value. This can be accomplished by means of BPSK indicator, in which the digital charge is decided by the outgoing signal's phase.[19] The input data combines in the MMI region with the correct signal phases to produce an output, what translates to logic 1, or eliminate signal creation, which correlates to logic 0 at output pin. The data structures can then be implemented by selecting the appropriate values in calculation to the phases of operation.[54]

6.1 *Logic Gates Based on Self-Collimation*

When a beam of light strikes a PhC structure with area, it transmits the signal to some extent. As a result, the phase of the reflected beam changes in relation to the beam splitter. The diameter of the dielectric material in the SC PhC zone affects the time delay. The reflected light lasers may interact effectively with another emitted light with the suitable phase. By changing the radii of the rods and producing varying phase shifts between the transmitted photons at the input sides, logic gates based on SC PhC was created. Numerous works have proven a full collection of the all the logic circuits using this method. The schematic construction of the plasmatic self-collimated device described by is shown in Fig. 29. Two inputting faces (I_1 and I_2) and two output stages make up this instrument (O_1 and O_2). By adding phase differences between two beams, it may function as OR and XOR processing elements (occurrence on the effort stages I_1 and I_2). The outlet faces O_1 and O_2 act as OR and XOR logic gates, correspondingly, if the phase shift between the intakes $1(I_1)$ and $2(I_2)$ is positioned to $2k\Pi/2$.

6.2 *Logic Gates Based on Multi-Mode Interference*

To create logic gates dependent on MMI, the input logic contents for each gate must be decided by the amplitude of the two inputs. This can be accomplished using BPSK signals, in which the standard logic value is decided by the output signal's amplitude rather than its phases.

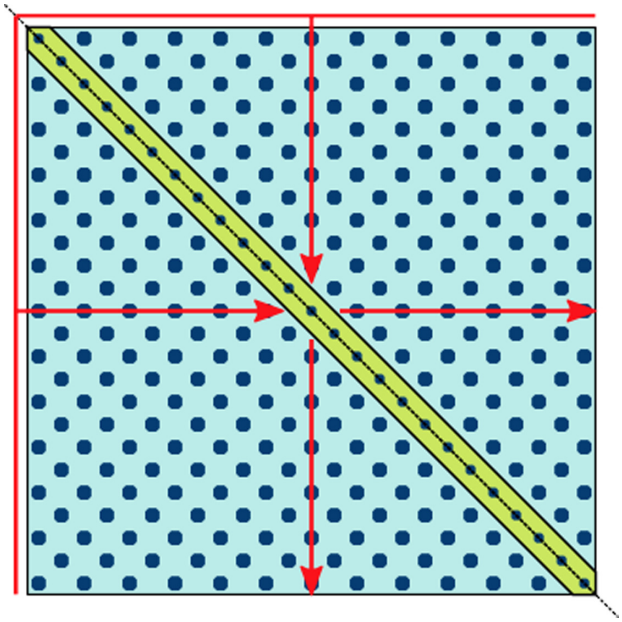

Fig. 29 Diagrammatic illustration of 13×13 PhC logical device based on self-collimated consequence.[19]

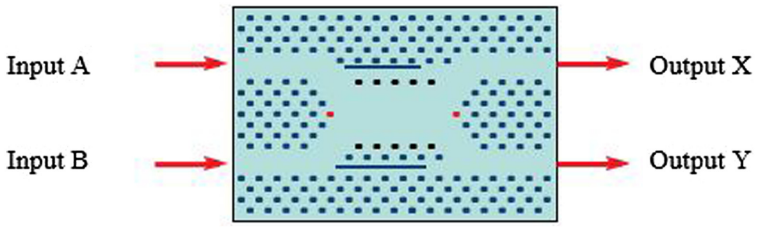

Fig. 30 Liu et al.[35] suggested a conceptual description of 17×10 PhC logic device based on multi-mode disturbance. Suitable rods are shown by red and black circles.[35]

The input signals combine in the MMI region with the correct signal phases to produce output signals, which translates to logic 1, or prohibit signal creation, which amounts to logic 0 at the output pin. The gates may then be achieved by selecting the appropriate characteristics in accordance to the stages of both the two inputs, as described by Ishizaka et al.[34,55]

Liu et al.[35] suggested the PhC MMI device, which is shown schematically in Fig. 30. It is made up of two inputs (A and B) and two output (C and D) ports (X and Y). Two types of BPSK pulses are inserted around each input pin to provide the rational functionalities. In the XNOR gate, logic 1 for input port A is represented by signal phase 0, whereas logic 0 is represented by signal phase. Logic 1 is defined at data phase $\Pi/2$ in input port B, while logic 0 is presented as signal component in input port B. Correspondingly, the XOR, OR, and NAND gates may be implemented by determining the amplitude of the suitable data signal for each circuitry.

6.3 *Logic Gates Based on Waveguide Interference Paths*

This is a straightforward, practical, and efficient method for projecting logic gates in optoelectronics. If diffraction pattern occurs between input beams, the large bandwidth condition (logic 1) is ensured in this design. This is done by creating a phase shift of $2k\Pi$ from input signals by constructing an intersection with a path difference of 0. In contrast, if the phase shift of $(2k\Pi + 1)$ is generated, resulting in two beams between the two inputs, resulting in the lower index condition (logic 0). Fu et al. theoretically realized the OR, XOR, NOT, XNOR, and NAND gates that use this technique.[47] The shapes were reflected onto a photonic dielectric with a

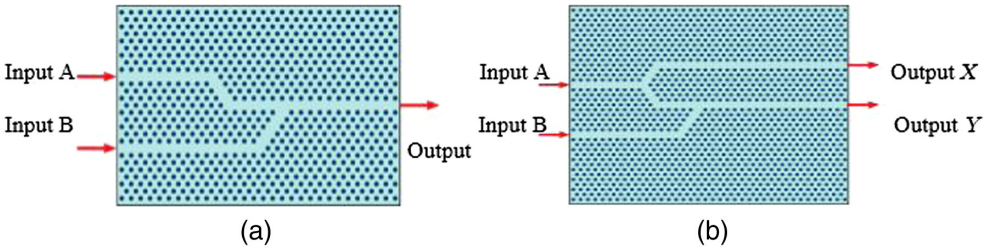

Fig. 31 Fu et al.[47] offered photonic diamond (a) 30×14 OR gate and (b) 40×20 XOR gate in a schematic diagram.[56]

refractive index of 11.56 made out of a triangular network of cylindrical si material inserted in an air background environment. The silicon rods' lattice parameter and thickness were 875 and 495 nm, accordingly. As shown in Fig. 31(a), the OR gate terminal is made up of two overlapping waveguides (inputs) at 10.5 nm to the cross waveguide connecting them, producing an inclination of 120 and a phase shift of 0. If a single photon is pumped through one of the ports, the great way to express can continue via the wavelength to the outputs, resulting in a logical value of 1 in the output. When light rays are instantaneously injected into both inputs, diffraction occurs, resulting in high maximum output. When no incident beam is pumped into any of input ports, no light is produced at the outputs, resulting in a logical negative number.

As shown in Fig. 31(b), the planned construction for the XOR gate comprises of two optical fibers with one parameter of path lengths connecting the other. So, when outputs are stimulated concurrently with a wideband source, a phase shift between the signals produces diffraction pattern, and the output current is close to zero (0.67%). When only one input is activated, the output voltage is more than 75%. The XOR logic gate was implemented by taking transmitters larger than 70% and receptions <1% as logic values 1 and 0. The NAND and XNOR gates were modeled in XOR technology, but with the addition of an input signals, provided a large transmission outcome when no signal was pumped into the inputs. As a result, propagation frequencies higher than 85% and <10% for logic values 1 and 0 have already been observed for all these systems. The suggested logic gates can operate in the wavelength 1550 nm and in the low-power region. The intensity contrasting ratio between both the digital signal for the processing state of 1 and 0 was also reported to be higher as 21 dB. A majority of logic gates have the same values.[56] The system allows building of simple and optimal computation circuits, while the latter is a logic gate device that is expected to be used to create circuits near the direct transition of computing. The authors found that transmission levels at the output is more than 85% and <36% may be regarded as logic 1 and 0, correspondingly, for the majority of logic gates. The comparable emission for the logic 1 was discovered to be as high as 40% for the Feynman gate, shown in Fig. 32(b), whereas transmitter's rates <10% corresponding to the logic 0.

D'souza and Mathew[44] showed the functioning of the XOR, NOT, OR, and AND logic gates using the control signal influence in a 2D PhC made of a square lattice of cylindrical silicon rods with a dielectric permittivity of 11.56 in a background environment of air. The lattice constant was 650 nm and the rod lengths were 230 nm. As shown in Fig. 33, the photonics are made up of a square ring resonator broadband with three additional linear diffraction gratings that are coupled by the resonant cavity. The signal pumped into the input optical fiber is divided in two

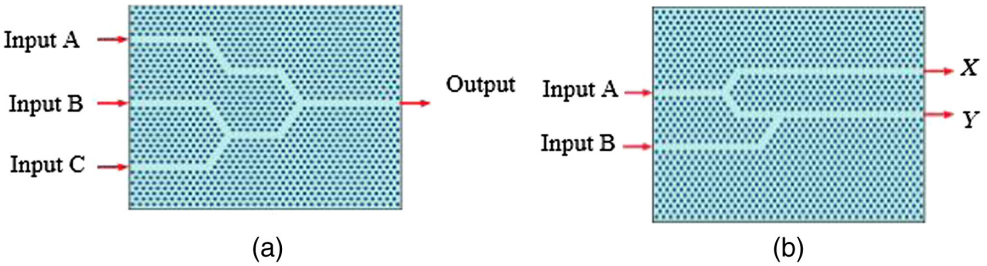

Fig. 32 (a) 40×20 Minority and (b) 38×20 Feynman gates for photo detectors.[56]

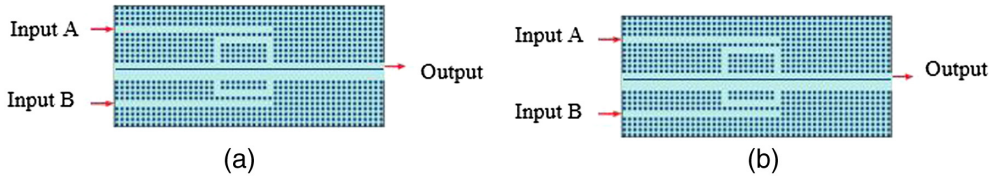

Fig. 33 Photonic crystalline (a) 52×23 AND gate and (b) 52×23 XOR gates in a designed circuit.[44]

by the resonant cavity. If there is shift in the phase, a higher output radiation is acquired at the output, and the OR, AND gates are implemented. The XOR and NOT logic gates have also been obtained when designing the ring resonator to create diffraction pattern. These systems have the benefit of being able to operate at a variety of frequencies within the 1550 nm. The authors mentioned that the dynamic range was more than 35 dB.

These electronics were subjected to a technique for evaluating the influence of structure disorder on nanostructure logic gates to decide their response time and low latency.[57] The approach was based on the assessment of two metrics: the error rate and the average absolute divergence error in communication. Matec evaluates the device's imperfection degree through the input impedance, and bit error rate is the probability that a produced nanostructure logic circuit does not perform its logic function correctly. The scientists discovered that locations in the edges and near to the outputs are more critical in systems with a triangular lattice. Hussein et al.[58] present novel in all-optical contain all logic gates having a square lattice. The patterns were created by embedding 2D square lattice optoelectronic crystalline phase of tungsten (Ge) rods with dielectric constants of 16 in an air background. The rods' radius was positioned to $0.15a$, where a is the crystal lattice parameter, and its value was chosen as 580 nm to provide a 1550-nm operating range. Figure 34 shows how an optical resonator is created and produces the interference effect needed to obtain the logical function. Optical transmission speeds of 3.8 to 7.6 Tbps and contrast ratios of 5.036 to 12.15 dB are available.

Figure 35 shows[25] achievement of a small PhC device that may work as a NAND or NOR logic gate. It is made up of a GaAs/AlGaAs nanostructures and a 2D pattern of triangular lattice in a PhC slab. The NAND or NOR gates can be made by altering target rods on the construction. According to the scientists' simulated data, the top power limit for representing logic 0 is 0.17 Pin, where Pin is the input power. On the other side, 0.50 Pin is discovered to be the lower limit for representing logic 1. The response speed of the NAND and NOR logic gates is 5 ps.

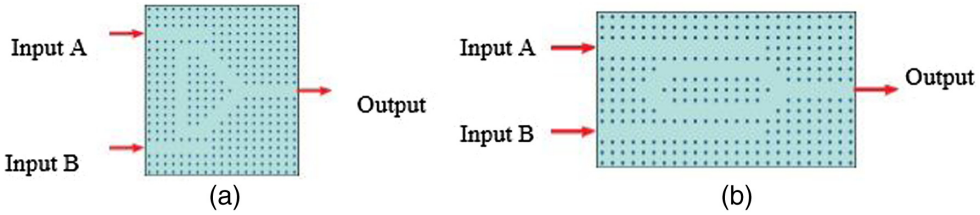

Fig. 34 Depiction of PhC (a) 19×21 AND gate and (b) 25×15 OR gates planned by Hussein et al.[58] Adapted from Ref. 58.

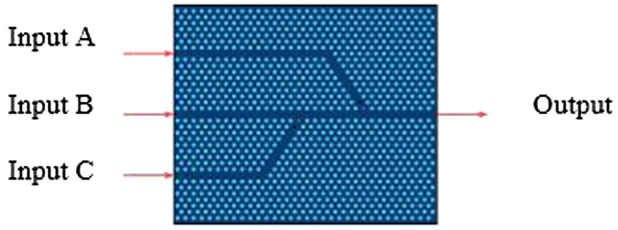

Fig. 35 The XY perspective of the 33×18 PhC compact system is depicted schematically.[25]

Fig. 36 A schematic illustration of 21×12 crystal switch.[27]

Dark and bright hues are represented by the dielectric constants 1 and 2, respectively. The red and black circles show the target rods in PhC structure that need to be improved to accomplish the NAND and NOR logic functionalities.[25]

6.4 *Logic Gates Based on Kerr Effect*

A waveguide-cavity linked system is constructed, and the interfaces must be suitably positioned to achieve logic circuits employing the Kerr phenomenon on PhC.

A high-contrast all-optical switching technique method is developed.[26] As shown in Fig. 36, the proposed mechanism is a 2D PhC made up of a lattice structure of dielectric rod ($n = 12.26$) in air. When the signal concentrated within the cavity is significantly larger, the cavity resonator is pulled down to the resonance frequencies, and the lower data condition is attained. A coupled mode was used to verify the instability's accuracy, and it showed great accord with FDTD experiments.

Nonlinear elements are shown by red line fragments[26] was used as a starting point. First, all-optical logic gates in optoelectronics were suggested in a subsequent study by the research organization.[27]

The construction is made up of two optical fibers, one for input and one for control, placed in a cross shape. In additional, as shown in Fig. 37, a cavity with immediate Kerr non-linearity was introduced in the waveguide's junction. Cross-talk between both the optical fiber is prevented in this design because their waves are parallel to their axes; as a result, each wavelength coupled to just the cylinder with much the same axis symmetrical. To demonstrate transistor functioning, FDTD simulations are conducted. When the intake and controller diffraction gratings are stimulated with selection of around 200 mm, the ON state is attained at 25 ps. The semiconductor is in the OFF state if just the inputs are deployed. The suggested structure's features were a modest dimension of a few micrometers square and a resource need of only just few milliwatts at a 10-Gbit/s switch velocity. Neisy et al. suggested an all optical double multiplexer based on PhC resonating chambers in their findings for useful functional devices.[28] A 31×31 square array of piezoelectric rods in air makes up the appropriate basis. As shown in Fig. 38, two input

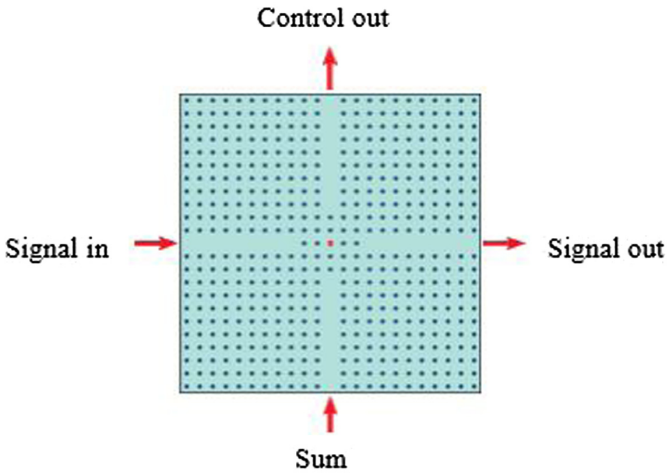

Fig. 37 A diagrammatic representation of 23×23 planned waveguide transistor.[27]

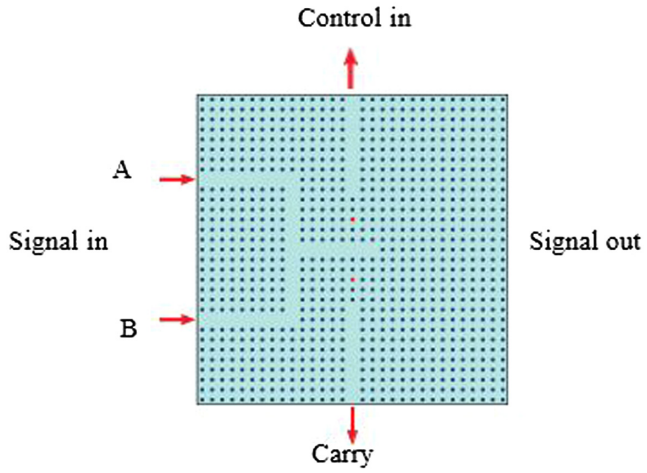

Fig. 38 The 31×31 plasmatic half multiplier[28] is depicted schematically.

waveguides and non-linear resonating cavities were added and tuned to achieve the desired resonant frequency behavior. A constant signal with a wavelength of 1553 nm and an infrared intensity of 10 mW/m^2 is utilized as an analog input to demonstrate half adder capability. Logic 1 and logic 0 were defined as values more than 70% and <5%, accordingly. The suggested structure's great benefits are its simplicity and low latency rates of roughly 3 ps

Dynamical materials are shown by red circles.[28] Alipour-Banaei and Seif-Dargahi projected it multiple optical 1-bit half-adders were cascaded to create the structure.[29] Inside a rod type, 2D lattice structure with lattice structure, the finished structure comprises of highly nonlinear resonating rings. The design has input diffraction gratings X, Y, and Z, and output beam splitters SUM and CARRY. The FDTD approach was used to verify the adder's effectiveness and functioning. Relatively stable propagation levels larger than 60% and <5% were classified as logic 1 and logic 0, correspondingly, according to the findings. In addition, a 1.5-s time delay and a 439-m^2 footprint were recorded. The heat transfer due to information loss is now an issue in logic circuit development and manufacturing. Landauer[30] demonstrated that network failure, which is an unavoidable phenomenon in irreparable logic circuits, causes a significant quantity of energy wastage inside wide scale circuits. However, due to the one-by-one translation between source and destination nodes in reverse logic circuits, it is possible to deduce the value of input pin from the output pins.

Cyclic substances are shown by red circles.[59] The ports for transmission as a result have no information loss and decreased energy dissipation. All-optical bidirectional XNOR and XOR gates dependent on microwave spreading in asymmetric photonic crystalline solids have been demonstrated.[59] Figure 39 shows the proposed electronics, which include two bridge waveguides functioning as outputs and inputs, and several linear and nonlinear defective rods. The basic

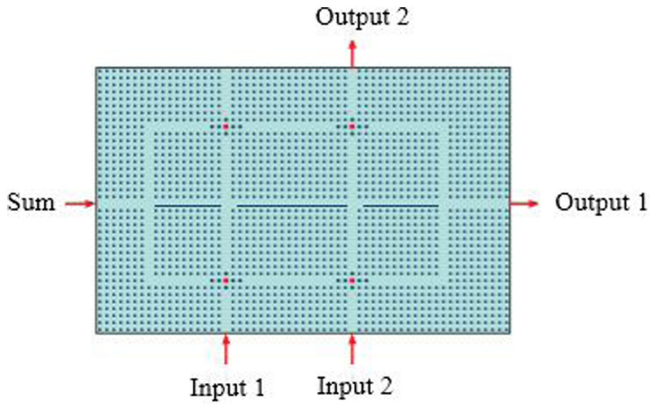

Fig. 39 PhC reversible 60×38 XNOR and XOR gates in a designed circuit.[59]

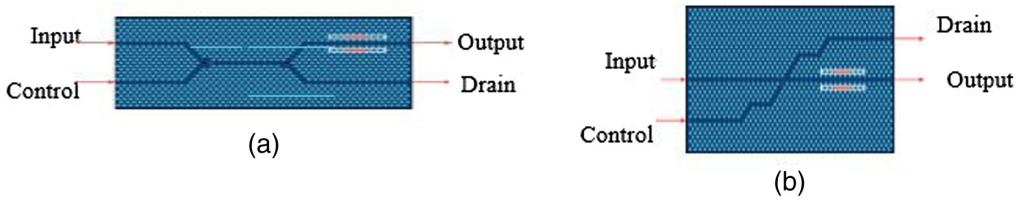

Fig. 40 (a) The *XY* vision of the 46 × 15 waveguide integrating switch *N* and (b) 45 × 18 switch *P* is depicted schematically.[62]

structure was a 2D PhC with an interference pattern. The XOR bidirectional logic is created by mapping one of the inputs to one of the outcomes and computing the normal binary operation. One waveguide is transferred to one of the outlets in the XNOR, while the traditional XNOR operation is done in the other. The outcomes demonstrated that the logic gates worked correctly for transmitting values of more than 65% and <2% which were referred to as logic 1 and logic 0, correspondingly. The creator observed a greatest time delay of 10 ps to obtain the response. Recently published a paper on complementing PhC combined logic circuits.[60] It is made up of two microcontrollers, switch *N*, and Switch *P*, as shown in Fig. 40. The latter is an AND gate that is similar to an N-type metal oxide semiconductor logic circuit. The latter may function as an integrator and a PMOS logic cell. The authors' simulation findings show a very resourceful clock rate of more than 20 GHz, ensuring process at about the same spectrum (about 1550 nm) at both source and load. They also discovered that the suggested devices have well-defined outputs voltage level that reflect the two logic states 1 and 0, and a CR of up to 6 dB. This enables the construction of silicon photonic ubiquitous digital logic, such as metal oxide semiconductor

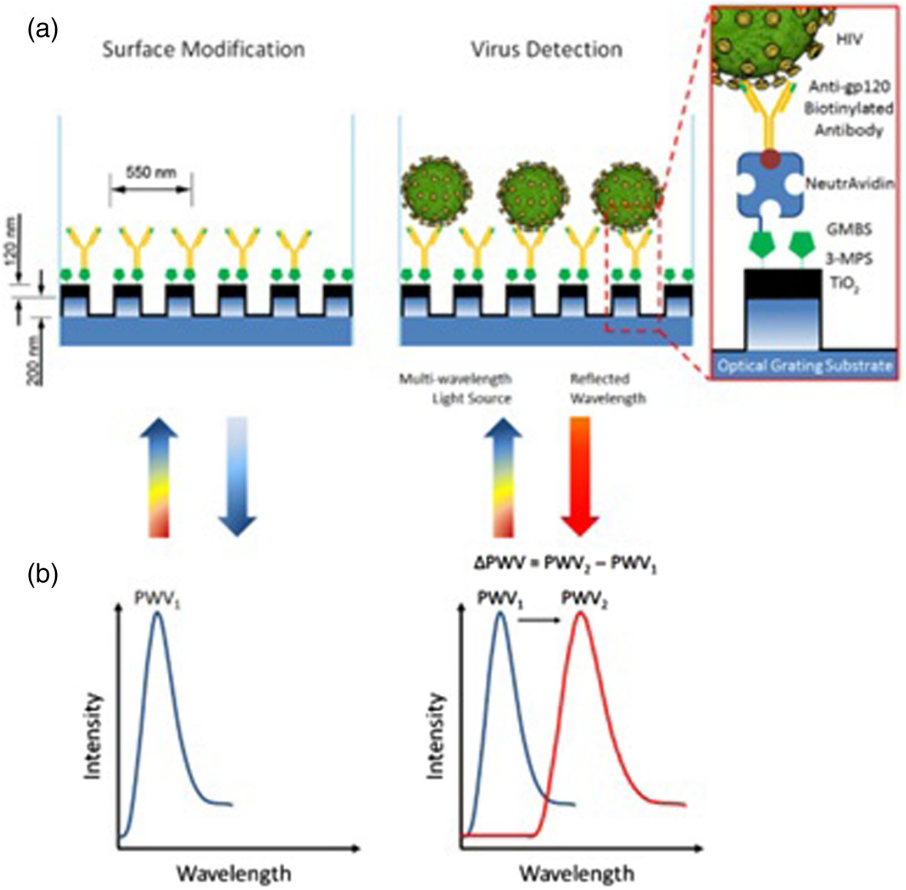

Fig. 41 Diagram of PhC based virus recognition stage.[64] (a) Surface Modification and Virus Detection (b) Intensity Vs Wavelength.

field effect transistor for electrical digital circuits, for the very first time, allowing for a higher processing abstraction level, allowing for the transition from fundamental elements to computer systems. Other approaches for PhC gates have now been considered as shown in Table 3. SOA, PhC fiber, resonator cavity, induced surface-enhanced Raman, and Mach–Zehnder spectrometer are some instances.[62,63]

Dark and bright lights are represented by the dielectric constants 1 and 2, correspondingly. Appropriate rods with radii of $0.75r$ and $0.5r$ are shown by black and red rectangles, correspondingly. $S_1 = 0.34a$, $S_2 = 0.27a$, and $S_3 = 0.13a$ are the movements of the rods around the structure. Adapted from Ref. 59. PhCs are alternatives for developing functional logic systems with low energy consumption, great efficiency, and fast data computing capabilities.

A nonlinear material's wavelength screen is coated with TiO_2 on the bottom surface of PhC sensors volumetric flasks. Binding occurrences within the near surroundings of the sensor field change the bulk RI, resulting in the highest point wavelength value of the scattered light. Rereleased from Ref. 64; and legally enforceable actions within the near surroundings of the sensor field modify the bulk RI, resulting in changes in the peak wavelength value of the mirror light as shown in Fig. 41. The binding of macromolecules and/or bivalents to the biosensors interface is directly proportional to the variation in maximum wavelength[64] is a reference.

7 Conclusion

An extensive overview of various PhC-based strategies for building all-optical logic gates is addressed, with comparisons made based on many characteristics, such as the CR, baud speed, and various areas with several limitations. Also, a literature overview of several ways to build PhC logic devices is discussed here. We discovered that the SC effect, MMI, waveguide interference, and nonlinear phenomena have all been used to successfully show PhC logic gates. We emphasize that each strategy is appropriate for certain applications based on its strengths and weaknesses. SC and MMI strategy, e.g., can be employed for minimalism and compact size strategy, as well as stage shifter and enhancers. Electronic circuits based on interference channels can help designers to create photonic computers with minimal power consumption and quick response times. Finally, asymmetrical PhC input signals can lead to development of computer chips by allowing creation of devices with a brightness and contrast level. We anticipate that with this study and the concerns mentioned here will be able to improve the progress of PhC-based logic circuits.

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