Substrate noise coupling: a pain for mixed-signal systems

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ABSTRACT

Crosstalk from digital to analog in mixed-signal ICs is recognized as one of the major roadblocks for systems-on-chip (SoC) in future CMOS technologies. This crosstalk mainly happens via the semiconducting silicon substrate, which is usually treated as a ground node by analog and RF designers. The substrate noise coupling problem leads more and more to malfunctioning or extra design iterations. One of the reasons is that the phenomenon of substrate noise coupling is difficult to model and hence difficult to understand. It can be caused by the switching of thousands or millions of gates and depends on layout details. From the generation side (the digital domain), coping with the large amount of noise generators can be solved by macromodeling. On the other hand, the impact of substrate noise on the analog circuits requires careful modeling at the level of transistors and parasitics of layout, power supply, package, PCB, … Comparison to measurements of macromodeling at the digital side and careful modeling at the analog side, shows that both the generation and the impact of substrate noise can be predicted with an accuracy of a few dB. In addition, this combination of macromodeling at the digital side and careful modeling at the analog side leads to an understanding of the problem, which can be used for digital low-noise design techniques to minimize the generation of noise, and substrate noise immune design of analog/RF circuits.

Keywords: Substrate noise coupling, mixed-signal, RF, analog, CMOS, scaling, crosstalk.

1. INTRODUCTION

CMOS technologies are subject to scaling. This is the fulfillment of Moore's law and the schedule of the implementation of this law is fixed in the International Technology Roadmap (ITRS) for semiconductors [1]. Downscaling leads to a speed increase for digital circuits, together with a reduction of size and energy consumption per operation. Although downscaling is accompanied with a degradation of analog performance parameters such as matching, 1/f noise, intrinsic gain, it also brings about an improvement of the performance of analog/RF circuits or, for a given set of specifications, a decrease of the power consumption. These improvements with downscaling for analog/RF are evidenced by the growing number of products that contain analog and RF functions, implemented entirely in CMOS [2][3].

For economical reasons, a single-chip implementation of mixed-signal systems such as wireless systems[1] is preferred over multi-chip solutions. Since scaling reduces the area and energy consumption per gate to ever decreasing quantities, it will give birth to mixed-signal systems where the number of analog components will shrink in favor of an increase of the digital circuitry: several functions that were traditionally reserved for analog circuits, are being taken over by digital circuitry. Moreover, analog impairments are being more and more compensated with digital signal processing techniques (e.g. calibration techniques, offset compensation, …). However, the remaining analog circuits will suffer from the effect of the switching activity of the digital circuitry. This switching causes a noisy signal that enters the substrate, which is common to the analog and digital part of the IC. Substrate noise causes a decrease of the signal-to-noise ratio for the analog circuits. Since it is a problem that is difficult to understand and to model, it may cause malfunctioning and extra design iterations.

The crosstalk problem of substrate noise is recognized in the ITRS roadmap as one of the most difficult challenges for scaled technologies. We illustrate the problem with two examples: the substrate noise generated by a 220 kgates digital circuit implemented in a 0.35 μm CMOS technology [4] and the output of a 3.5 GHz voltage-controlled oscillator (VCO), designed in a 0.18 μm CMOS process, in the presence of a disturbance in the substrate [5].

[1] A single-chip system is often a subsystem of a complete system: the latter contains a crystal, RF filters, power devices, antenna switch, …

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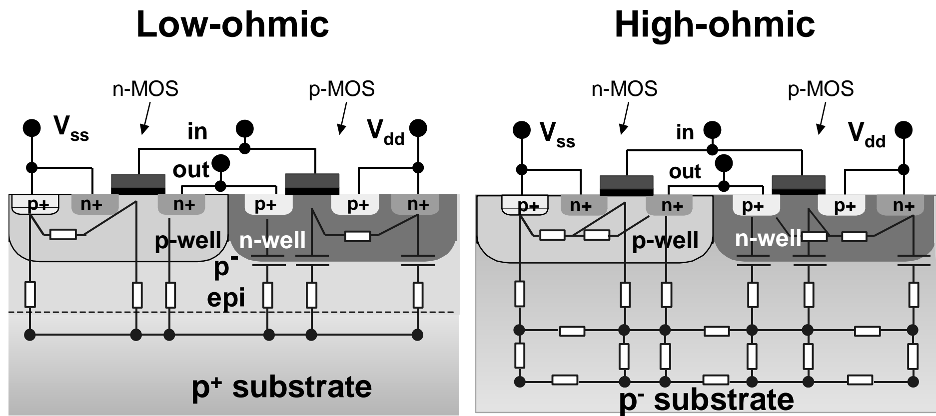

Figure 1: simplified cross-section of a digital CMOS inverter, realized in two substrate types: (left) a highly doped, low-ohmic substrate (resistivity well below 1 Ω.cm) with a lowly doped epitaxial layer on top; (right) a high-ohmic substrate (resistivity in the order of 10 Ω.cm). The latter is mostly used nowadays.

The 0.35 μm CMOS 220 kgates design has been realized on a highly doped, low-ohmic substrate (Figure 1 left). The operation of this circuit generates switching noise which, depending on the clock frequency, can rise up to 340 mV peak-to-peak, as evidenced by the measurements shown in Figure 2. To have an idea about the consequences of such substrate noise disturbance, consider a 10 bit analog-to-digital that would be put on the same chip. If a full-scale signal for this converter corresponds to a peak-to-peak voltage of 1.3 V, then a suppression of well below 48 dB is required for the generated noise signal if one wants to prevent the substrate noise aversely affecting the dynamic range of the converter. An important challenge during the design of the digital part of an IC is to predict the amount of generated substrate noise, such that a specification can be set on the suppression of this noise.

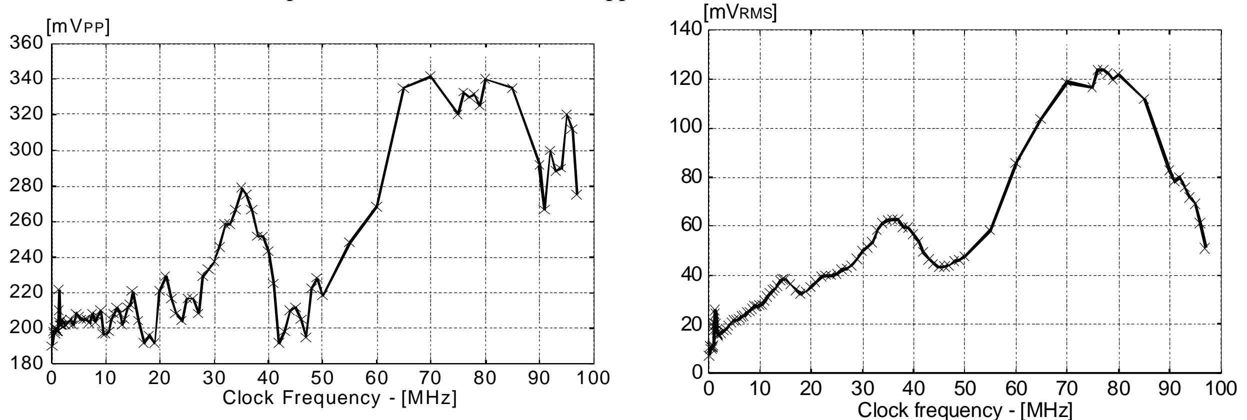

Figure 2: substrate noise generated by a 0.35 μm CMOS 220 kgates digital circuit. Left: peak voltage of the substrate noise as a function of clock frequency. Right: RMS voltage of the substrate noise as a function of clock frequency.

As a second example, we consider the measured response of a 3.5 GHz 0.18 μm CMOS voltage-controlled oscillator (VCO) in the presence of a disturbance in the substrate, which is high-ohmic in this case (Figure 1 right). When a disturbing 10 MHz signal is present in the substrate (Figure 3 left), this can enter the circuit via different ways. One of these is the parasitic resistance of the ground lines (Z_{GND} in Figure 3), that are connected to the substrate via many contacts. Once the disturbance is present in the circuit, it will affect the circuit. For the VCO, this occurs as sidebands at a frequency offset of ±10 MHz from the carrier (see Figure 3 right). The challenge in the design of an analog/RF circuit

is to predict how a given substrate noise disturbance affects the operation of this circuit, hereby taking into account parasitics such as ground line resistance and couplings from the substrate to active and passive components in the circuit.

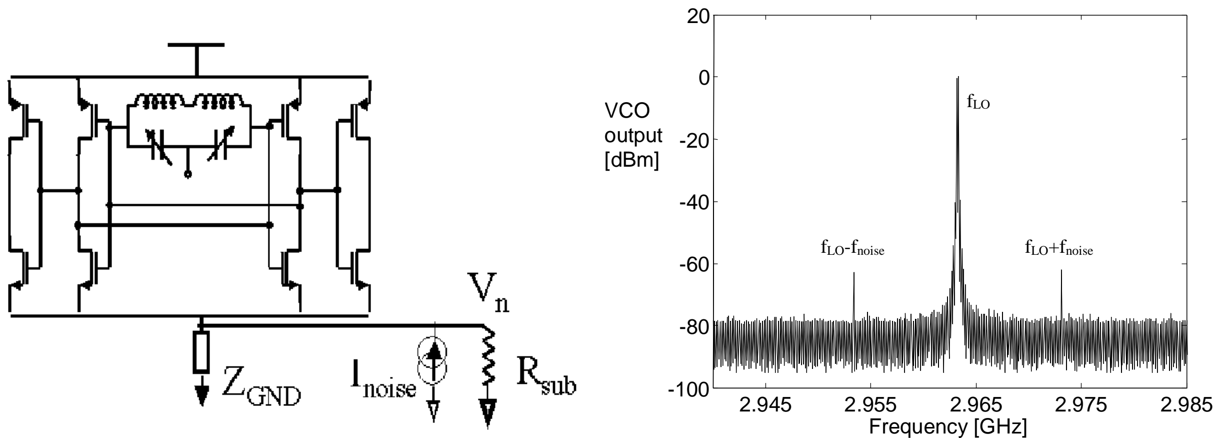

Figure 3: (left) schematic of a 0.18 µm CMOS 3.5 GHz VCO in the presence of a disturbance in the substrate (simply modeled with I_{noise} and R_{sub}); (right) measured spectrum at the output of this VCO when a signal at a frequency of 10 MHz is entered into the substrate.

The problem of substrate noise coupling is a very complicated one: it is caused by a multitude of switching digital gates, while the way in which it affects the analog/RF circuitry, the so-called impact, is caused by layout details. Therefore, this problem is best split into three different parts: generation of the substrate noise, propagation through the substrate and impact onto the analog/RF circuits.

First, there is the aspect of the noise generation in the digital circuitry. As will be discussed below, a prediction of the amount of generated noise with reasonable accuracy requires macromodeling at a higher level than the transistor level, since a detailed circuit-level simulation of the noise generation is only feasible in a reasonable time for very small designs, with a gate count below 1,000. Such macromodeling requires a good understanding of the different generation mechanisms of substrate noise. These mechanisms are discussed in Section 2. In combination with a model for the assembly parasitics, substrate noise generation macromodels can predict substrate noise in digital circuits of realistic size with accuracies of about 20 % compared to measurements, as will be discussed in Section 3. Once it is possible to predict the generated noise, different design techniques at the digital side can be evaluated to lower the amount of generated noise. A few of these design techniques are discussed in Section 4.

Next, there is the propagation of the noise through the substrate. To model this, there exist several programs [6][7][8] that generate a threedimensional resistive or RC network for the substrate. In low-ohmic substrates, which are common for technology generations of 0.35 µm and above, the substrate is often simplified to one single node (see Figure 1 left). Such simplification cannot be made for high-ohmic substrates (see Figure 1 right), which attenuate more than low-ohmic ones. High-ohmic substrates are more used nowadays than low-ohmic ones.

Finally, there is the aspect of impact of substrate noise on analog and RF circuits. Here, a careful modeling of the assembly characteristics, layout details, … is required to bring simulations and measurements in agreement. As will be shown in Section 5, substrate noise often impacts the analog circuits via different ways. If these are not well modeled, then it is not clear during circuit design how this impact can be suppressed.

2. SUBSTRATE NOISE GENERATION MECHANISMS

There exist three mechanisms that generate substrate noise [9]. The first mechanism is caused by impact ionization: hot electrons that travel from source to drain in a switching n-MOS transistor create hole-electron pairs. The resulting hole

current flows into the substrate. The second mechanism is the current injected into the bulk of a transistor via its drain-bulk or source-bulk junctions when the voltage at the drain/source switches. It can be shown [9] that in nowadays' and future CMOS technologies (with a high-ohmic substrate) these two mechanisms are negligible compared to the third mechanism, which is bounce on the digital supply lines that is injected into the substrate via many ground contacts.
The injection of digital ground bounce into the substrate can be understood using the equivalent circuit (see Figure 4) of a digital circuit where a switching event occurs. When the output of the switching gate goes from a logical 1 to a logical 0, then the capacitance C_{og} between the output of that gate and ground is discharged while the capacitance C_{op} between the output and V_{DD} is charged. This causes a supply current to flow.

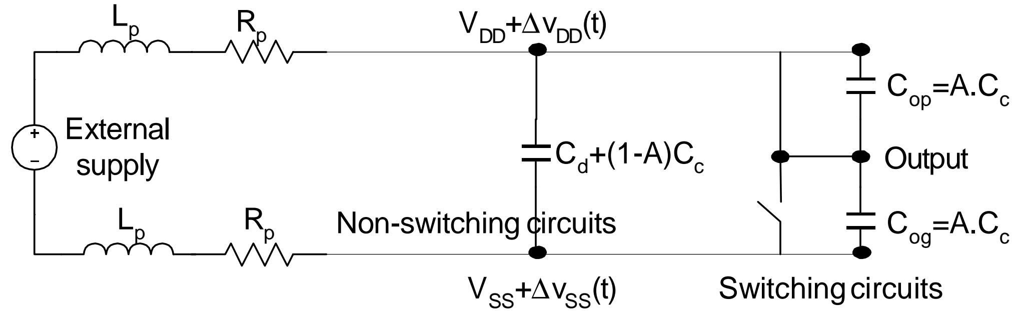

Figure 4: generation of bounce on the digital supply lines due to switching of a part of the digital circuit.

In large digital circuits, high peaks of the supply current create power-supply-line noise in the supply network due to the RLC network formed by the chip capacitance C_c and the decoupling capacitance C_d between V_{DD} and V_{SS}, the package inductance L_p of the power and ground connections, and the series resistance R_p in these connections. In a p-type substrate this supply noise couples capacitively into the substrate from V_{DD} via the n-well junction capacitance, and resistively from V_{SS} via the substrate contacts. The circuit capacitance C_c can be divided in two parts: a switching and a non-switching one: $A \cdot C_c$ is the switching portion of this capacitance where A is the switching activity factor of the circuit, which is typically between 0.05 and 0.30 for telecommunication circuits. $\Delta V_{DD}(t)$ and $\Delta V_{SS}(t)$ are the noise on the supply and the ground, respectively. We define t_c as the total duration of the current charging the switching capacitance.
In digital circuits of realistic size, the non-switching circuits and decoupling provide most of the current required by the switching circuits. In that case, one finds for the maximum value of the ground noise, which is obtained at $t = t_c/2$:

$$\Delta V_{SS}(t = t_c/2) = \frac{1}{2} \frac{A.V_{DD}.C_c}{C_d + C_c} \tag{1}$$

This noise is injected into the substrate and can propagate to the analog circuitry.
Equation (1) suggests that a smaller ratio of the switching capacitance to the non-switching capacitance in large digital circuits is useful for noise reduction. Further, reducing the inductance will not reduce the peak value of the power-supply-noise.

3. MACROMODELING OF THE GENERATION OF SUBSTRATE NOISE

A circuit-level simulation of the generation of substrate noise would require a transient simulation (e.g. with SPICE or SPECTRE) of the digital circuit extended with a model for the substrate. Such simulations can only be performed in a reasonable CPU time for digital circuits of very limited size (< 1,000 gates).
To tackle the complexity of the generation problem, different strategies have been presented [10-15] to model the generation of substrate noise at the gate level. The idea is as follows: a gate or standard cell is modeled by one or more current sources and some passive components. The current sources model (one of) the generation mechanisms that have been described in Section 2. The passive components are usually linear, and they model the circuit capacitance between the digital V_{DD} and ground, the n-well capacitances, resistances of the epi-layer underneath a standard cell for a low-ohmic substrate, ….
For example, the approach of [15] uses a macromodeling approach to deal with standard cell designs in high-ohmic substrates, as an extension of the modeling with low-ohmic, epi-type substrates [14]. In high-ohmic substrates, only the digital ground bounce needs to be taken into account as substrate noise generation mechanism, as mentioned in

Section 2. This ground bounce is caused by the supply current, which is modeled for each standard cell by a current source between V_{DD} and V_{SS}. The model is completed with an admittance in parallel with the current source. This source is only active when the standard cell is switching. In standard cell designs, the cells are usually placed into different a few power domains, i.e. collections of cells that are connected to one single V_{DD} and V_{SS}. To macromodel each power domain, the model of each standard cell of a domain is connected to the same V_{DD} and V_{SS}, which in turn are connected to a package model that includes bondwire inductances and damping resistances. This model (see Figure 5) is completed with a substrate mesh connecting the on-chip power grid to the substrate.

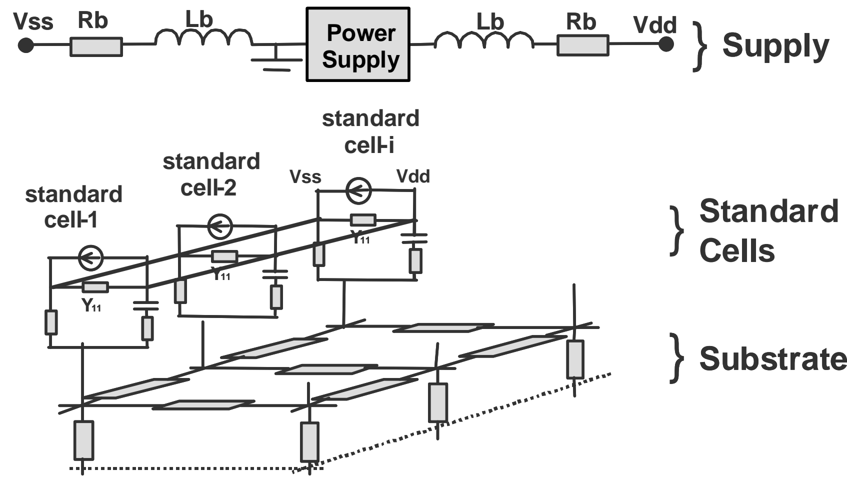

Figure 5: Macromodel of a power domain in standard cell-based digital circuit. This model is used for simulating substrate noise generation in high-ohmic substrates with the approach of [15].

In high-ohmic substrates the injection of current into the substrate underneath a digital gate can be neglected. One only has to take into account the bounce on the supply lines caused by the switching of a standard cell. This bounce is not zero due to the impedance of the assembly parasitics, which are modeled as well.

A computation of the generation of substrate noise then proceeds as follows (see Figure 6): prior to simulation a macromodel is constructed for every standard cell of the library.

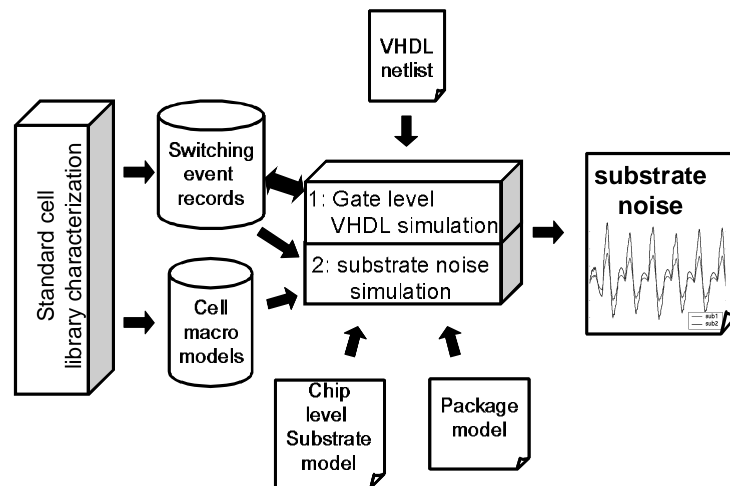

Figure 6: Substrate noise generation analysis flow. First, a gate-level simulation is performed. This determines for every standard cell the moments at which it is switching. At these moments, the current source of the macromodel of the standard cell is active. Next, this information is used in a time-domain simulation which comprises the standard cell macromodels as well as a model for the substrate and the package.

This modeling step only needs to be done once. Layout variations, which lead to different capacitances of the interconnections between the standard cells, are added afterwards for the circuit under consideration. Next, a gate-level simulation is performed. This gives for each standard cell the exact moment at which it is switching. Finally, a time-domain simulation is performed, where the standard cell models are combined with a substrate model and a package model. This simulation yields the waveforms of the substrate noise.
The accuracy of this approach has been verified with measurements on a 40K gates telecom circuit (circuit L1 in Figure 7), fabricated in a 0.18 µm CMOS process on a high-ohmic substrate with 18 Ωcm resistivity. It contains a 20-bit maximum-length-sequence Pseudo-Random-Binary-Sequencer (PRBS) circuit driving two cascaded sets of the IQ modulator and demodulator chains.

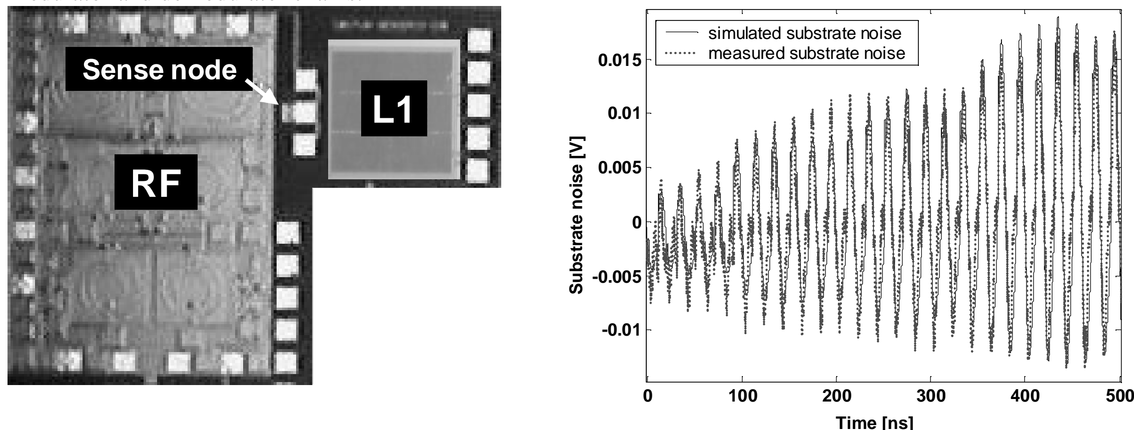

Figure 7: (left) Microphotograph of the test circuit (L1), 40K gates telecom circuit and the analog victim with the sense node in between; (right) comparison between a simulation of substrate noise using macromodels and measured substrate noise at the sense node.

In the right part of Figure 7, a comparison of the measured versus simulated substrate noise voltage at the sense node is shown. The digital circuit is clocked at 50 MHz, which is close to the resonance frequency of the package (approximately 55 MHz) to maximize the substrate noise voltage (for the experiment's sake). The first 25 clock cycles after end of reset have been plotted. Clearly visible is the start-up of the PRBS that gradually increases the activity of the circuit. The RMS value of the measured substrate noise is 6.5 mV, of the simulated waveform 7.7 mV, an error of 20%.

4. TACKLING THE SOURCE OF THE PROBLEM: DIGITAL LOW-NOISE DESIGN

In the previous section, we have seen how macromodeling can be used to predict the amount of generated noise. The next step is to reduce this noise by clever design. To this end, one should realize that in high-ohmic substrates the spectrum of the noise voltage somewhere in the substrate is proportional to the spectrum of the ground bounce in a digital power domain, as ground bounce in the dominant substrate noise generating mechanism. This ground bounce is the product of the spectrum of the power supply current of a digital power domain and the transfer function from this current to the digital V_{SS} (see Figure 8). In order to design a digital circuit for lower substrate noise generation, one can try to reduce either of the two factors in this product. We first consider these two factors in somewhat more detail.
The transfer function from the supply current to the digital V_{SS} shows a peak due to the resonance between the assembly inductance and the capacitance from the circuit itself and the decoupling:

$$f_{res} = \frac{1}{2\pi\sqrt{L_p \cdot (C_c + C_d)}} \tag{2}$$

In which L_p, C_c and C_d have been defined in Figure 4. In order to have an idea about the spectrum of the supply current, we first consider what typically happens in a clock cycle of a synchronous digital circuit. At the beginning of a cycle, flip-flops are switching, after which combinatorial logic is processing new data. As a result of these actions, the time-

domain representation of the power supply current in a single clock cycle can be approximated by a triangular waveform (see Figure 9). The Fourier transform of one such triangle is given by

$$
\begin{aligned}
I(\omega) &= \frac{Ip}{(j\omega)^2}\left[\frac{1}{tr}\left(1-e^{j.w.tr}\right)+\frac{1}{tf}\left(1-e^{-j.w.tf}\right)\right].e^{-j.\omega.tr} \\
\left|I(\omega)\right| &= \frac{Ip}{tr.tf.\omega^2}\sqrt{\left(tf.\sin(\omega.tr)-tr.\sin(\omega.tf)\right)^2+\left(tf.(1-\cos(\omega.tr))+tr.(1-\cos(\omega.tf))\right)^2}
\end{aligned}
\tag{3}
$$

with $\omega = 2\pi f$.

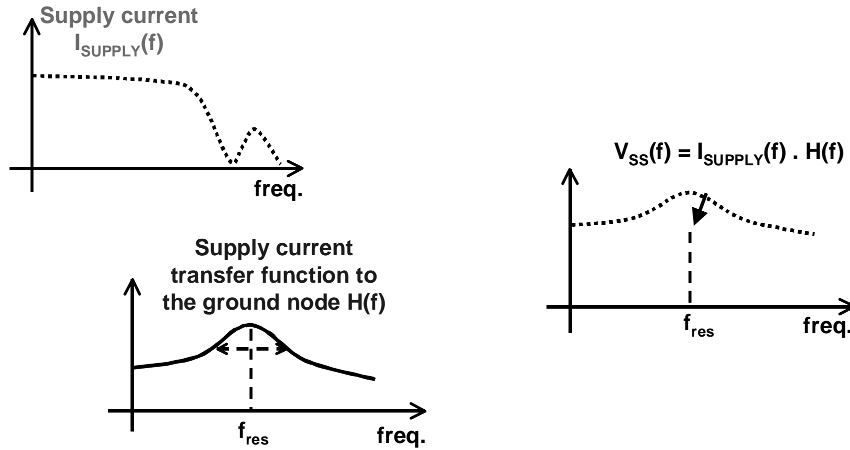

Figure 8: the spectrum of the voltage at some place in the substrate depends on the ground bounce. The spectrum of this bounce is the product of the spectrum of the supply current and the transfer function from the supply current to the digital ground V_{SS}.

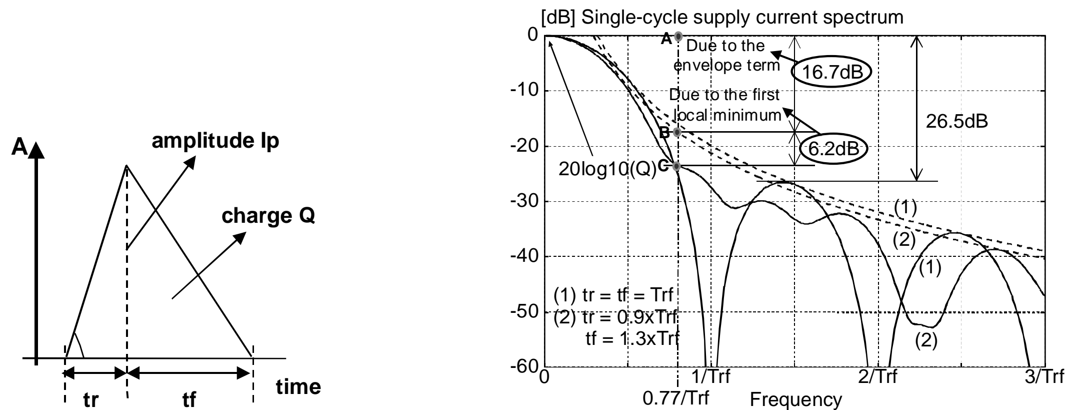

Figure 9: (left) the time-domain waveform of the supply current in a digital synchronous circuit can be approximated by a periodic repetition at the clock rate of a triangular shape with rise time *tr*, fall time *tf* and maximum *Ip*; (right) spectrum of the waveform on the left, corresponding to the spectrum of a single-cycle supply current waveform. The dotted line indicates the envelope, which follows a $1/f^2$ behavior (see equation (3)).

The magnitude of this spectrum is shown in Figure 9 with $tr = tf = Trf$. At a frequency $fc = 1/Trf$, it has a first local minimum, which is a notch in this case. Such notch occurs whenever the ratio of *tr* and *tf* is a rational number. Since the

envelope of the spectrum (dotted line in Figure 9 right) is given by $2.Ip.(tr+tf)/(\omega^2.Trf^2)$, the second lobe has a 26.5 dB smaller amplitude than the DC point. While an incremental change in *tr* and/or *tf* can shift the notch point, a main lobe remains present. In addition to the attenuation due to the fact that the envelope is a decreasing function of frequency, at the end of the main lobe (at frequency *fc*) the “oscillating” term provides an extra attenuation with a factor $sin(\alpha.\pi)/(1+\alpha)$, with α equal to *min(tr,tf)/max(tr,tf)*. As an example, for *tr* and *tf* equal to *0.9Trf* and *1.3Trf*, respectively, *fc* becomes *0.77/Trf*. At that point, the total attenuation of 22.9 dB consists of an envelope attenuation of 16.7 dBA and an extra attenuation of 6.2 dBA while the notch point occurs at *10/Trf*.
In a synchronous system, the power supply current can be approximated by a periodic repetition of the triangular waveform. This yields a discrete, sampled version of the spectrum in the right part of Figure 9, where the spectral lines are at the harmonics of the clock frequency. The deviation from periodicity of the power supply current causes a “noisy” contribution in between the spectral lines. This is demonstrated in Figure 10, which compares the spectrum of the ensemble average of the supply current to the spectrum of the actual SPICE-simulated supply current of a 100 gates circuit for a period of 3 ns (top) and 30 ns (bottom).

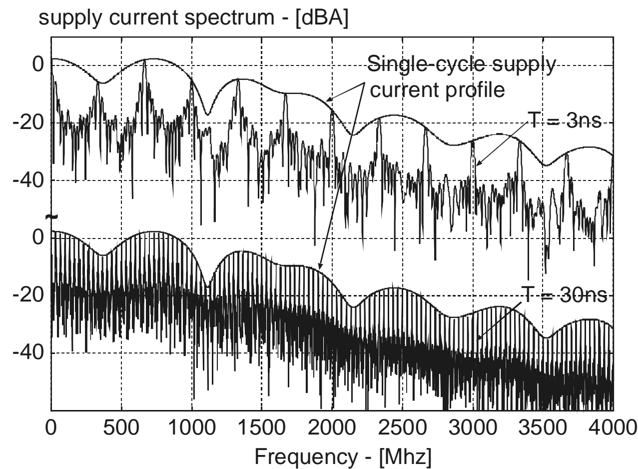

Figure 10: The spectra of the total supply current and the ensemble averaged supply current of a 100 gates circuit for a period of 3 ns (top) and 30 ns (bottom).

Equation (3) indicates that the notch point in the spectrum of the supply current shifts to higher frequencies when the rise and fall times decrease. This means that for a digital circuit with a given clock frequency, the low-frequency contents of the supply current grows with downscaling, as CMOS gates become intrinsically faster.
Having studied the general shape of both the supply current spectrum and the transfer function from that current to the substrate or to the digital V_{SS}, we next consider different ways to lower either of these values.

4.1. Reduction of the supply current transfer function

To reduce the supply current transfer function, one could increase the amount of decoupling capacitance, as already been pointed with equation (1). Further, one can try to increase the isolation from the substrate. This can be obtained by increasing the resistivity of the substrate. However, this is usually not an option, as it cannot be freely chosen by designers and, moreover, for bulk CMOS processes with a high-ohmic substrate, it does not change much with scaling. Another approach to reduce the supply current transfer function, used e.g. in [16], is to use standard cells with a separate bias for the substrate and the n-wells. All these solutions, although they are effective, increase the area and/or cost.

4.2. Reduction of the spectrum of the supply current

If a reduction of the supply current transfer function is a too expensive solution, one can try to the shape the spectrum of the power supply current, which is the leftmost factor in Figure 8. Several supply shaping techniques have been demonstrated to reduce the amount of generated substrate noise [16][17]. For example, in [16] a dual supply has been used for a design in a 0.35 μm CMOS technology with an epi-type low-ohmic substrate: the supply with a lower voltage is used for the cells that are not in the critical path and the other with the nominal supply voltage is used for the cells in

the critical path. In this way, the charge Q (see left) that is transferred at each cycle, is reduced. In combination with extra on-chip decoupling capacitance and the use of separate bias for the substrate and the n-wells, the RMS value of the substrate voltage has been reduced from 33 mV for a reference design in this technology to 11.5 mV. However, the extra decoupling and the larger size of the standard cells have increased the chip size with 72 %.
Another supply shaping technique is the use of intentional clock skew [16][17] to increase *tr* and *tf*. From equation (3) we can see that this shifts the main lobe in the frequency spectrum of the supply current to lower frequencies. This can be achieved by introducing different skews to the branches of a clock tree driving a synchronous digital circuit. To this end, the design is split into several clock regions and introducing skews for each clock region. In addition, a clock delay line is required, which generates a separate clock for every clock region. Using intentional clock skew one can shift the end of the main lobe or the notch in the supply current spectrum to a frequency below the resonance frequency f_{res}. This yields a reduction of the substrate noise, as illustrated in Figure 11.

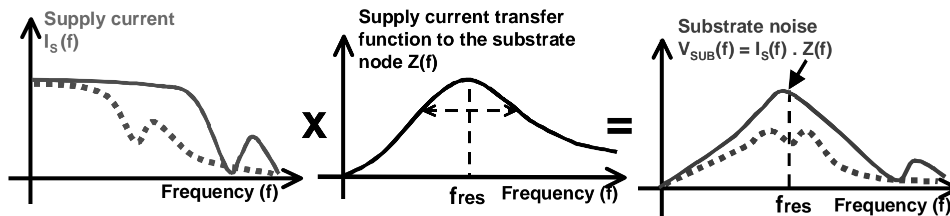

Figure 11: effect of intentional clock skew on the spectrum of the substrate noise. Solid lines correspond to the situation without skew. With clock skew one can shift the notch in the supply current spectrum to the resonance frequency f_{res} of the assembly inductance and the circuit/decoupling capacitance, yielding a lower substrate noise (dotted line).

This approach has been verified experimentally in [16], where a reduction of the generated substrate noise with a factor two has been reported, with a negligible penalty in power (4% more) and area (3% more)..
A further reduction of the supply current spectrum can be obtained by introducing frequency modulation (FM) on the clock [17]. This spreads the energy of the spectral peaks into side lobes such that the height of the peaks is reduced, while maintaining the same power. The bandwidth of these side lobes grows by increasing harmonics of the clock. For even spreading of these peaks as well as the peak at the fundamental clock frequency, the best choice for the modulation appears to be a triangular waveform with a modulation index greater than five. The frequency intervals in between these lobes can be used for as the frequency bands of operation for analog and RF circuits. Figure 12 illustrates the effect of intentional clock skew in combination with FM on the clock to reduce the spectral peaks in the supply current. When this combination is applied to the 40 kgates telecom circuit of Figure 7 left, a reduction of 26 dB is obtained for the ground bounce spectrum in the vicinity of the resonance frequency f_{res}.

5. IMPACT OF SUBSTRATE NOISE ON ANALOG/RF CIRCUITS

It is very important to know how a given spectrum of substrate noise affects the analog/RF circuits. If this cannot be predicted, then this may lead to conservative designs or malfunctioning analog/RF circuits. There exist a few design approaches that are generally accepted as being beneficial for low impact of substrate noise. Examples of such approaches are differential analog/RF designs, use of guard rings and triple wells, … We now briefly discuss these issues.
For analog circuits subject to substrate noise, differential design might be beneficial as the substrate noise disturbance can often be considered as a common-mode disturbance, which is suppressed in a differential circuit with a high common-mode rejection ratio.
In modern CMOS technologies the use of triple wells is a standard option. This allows to put an n-MOS transistor into a separate p-well, which in turn can be embedded inside a deep n-well. In this way, the bulk of the n-MOS transistor is now isolated from the substrate, at least at low frequencies [18]. At high frequencies (in the GHz range), the isolation effect is reduced [19] due coupling via the junction capacitors.

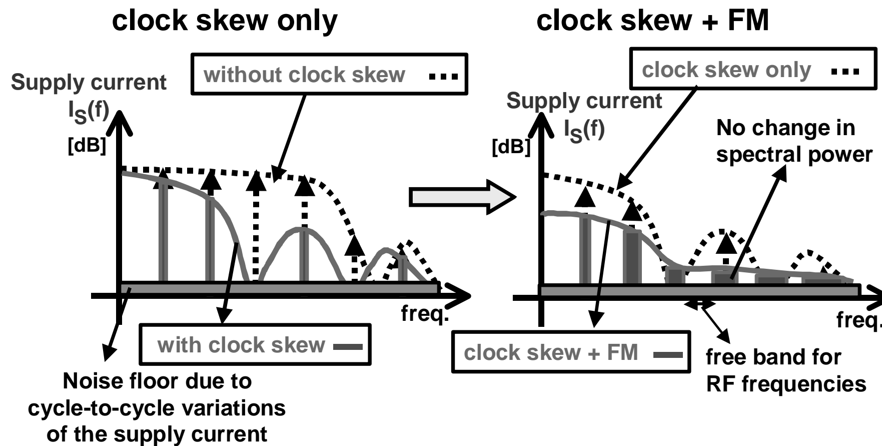

Figure 12: combination of intentional skew and FM on the clock to reduce the spectrum of the supply current.

Guard rings (Figure 13) provide another way to reduce impact of substrate noise on analog circuits. The principle is as follows: a highly-doped p-type ring that is connected to a quiet ground can collect the disturbances in the substrate before they reach the analog circuitry. Alternatively, an n-type ring can be put either around the analog circuit or around the digital circuit that generates the noise. The latter ring serves as a barrier for the noisy signals in the substrate rather than as a trap. The use of guard rings is being studied extensively [18-22]. In some cases, they can increase the isolation with 40 dB [22]. However, their effectiveness depends on their size, width, operating frequency, and substrate type. For example, in a low-ohmic substrate with an epitaxial layer, their effect is small, since their action is short-circuited by the high conductivity of the substrate. In a high-ohmic substrate, a p-type guard ring (Figure 13) seems to the give the best suppression [22].

The approaches mentioned in the previous paragraphs do not automatically lead to a sufficient suppression of substrate noise. A first reason is that the effect of these approaches is difficult to quantify. Next, their effect can be masked by the impact via a way that has been overlooked. For example, a guard ring might be useless if it is not connected to a quiet ground via a very low impedance. However, in nowadays' designs attempts for reduction of impact of substrate noise often come down to a blind application of these design approaches. The real effect of these approaches on substrate noise impact reduction are indeed difficult to predict.

The reason why substrate noise impact is difficult to predict, is that it depends on many details, that highly depend on the layout of the analog circuit. For example, as the substrate is usually tightly connected to the on-chip ground of the analog circuit via many substrate contacts, noise can enter the circuit via ground lines and cause impact due to the resistivity of these ground lines and the impedance between the on-chip ground and the off-chip ground [5]. Another possible entry point of substrate noise is the metal interconnect in general [23] and passive components [5].

Substrate noise caused by digital switching activity is not a big problem for every analog circuit. For example, the work in [24] studies the impact of substrate noise from a digital circuit with a 130 MHz clock on a 5 GHz low-noise amplifier (LNA), which are together put on a chip fabricated in a 0.18 μm CMOS technology with a high-ohmic substrate. Here the impact on the LNA is small since the LNA behaves as an almost linear circuit that operates at a frequency that corresponds to the 38th harmonic of the clock frequency, which is very small. In LNAs that have been designed in technologies with a low-ohmic substrate, impact can be higher: here one can even observe at the output a significant intermodulation product of the substrate noise component at the digital clock frequency (which is less suppressed than in a high-ohmic substrate) and the signal of interest [25]. Further, LNAs can be susceptible for strong signals at RF frequencies from other RF circuits, such as local oscillator signals, power amplifiers, … These RF signals can propagate through the substrate. Substrate coupling at RF frequencies caused by other analog/RF blocks, although not extensively discussed in this paper, can cause unexpected problems as well. For example, in a downconversion section consisting of a local oscillator (LO), mixer and LNA, the LO signal at the LO input of the mixer can propagate through the substrate to the LNA, where it is amplified and presented to the other mixer input. In this way, the mixer will produce DC offset, due to the mixing of two signals at the LO frequency [8].

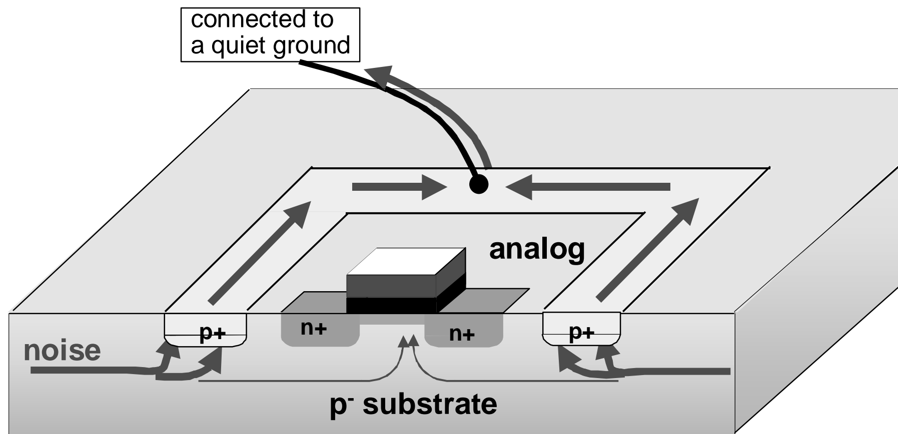

Figure 13: principle of a guard ring around an analog circuit to protect this against substrate noise.

Another analog circuit that can be affected by substrate noise is the analog-to-digital converter, as already mentioned in the introduction. Here, the comparators could take a wrong decision due to the presence of a noisy signal in the substrate [26].

An RF circuit that is sensitive for substrate noise from digital circuitry, is a VCO. This is an inherent nonlinear circuit, in which low-frequency substrate noise can be upconverted to sidebands in the vicinity of the oscillation frequency. This circuit has been studied extensively in [5] with the topology of Figure 3, oscillating at 3.5 GHz. In a VCO, the impact of substrate noise happens as follows: the disturbance propagates through the substrate and enters the circuit via different entry ports, such as the bulk of the transistors, the ground and power supply lines, the variable capacitors and inductors in the LC tank of the VCO, …Once a disturbance is present in the circuit, this disturbance can modulate the frequency. For example, the disturbance can modulate the voltage over the variable capacitor in the tank. This occurs at the output as narrowband FM, which is seen as sidebands in the spectrum close to the oscillator frequency.

A detailed modeling of substrate noise impact on the 3.5 GHz VCO requires the combination of circuit insight, together with circuit-level simulations of the VCO that is extended with models for the substrate, which can be extracted e.g. with "Substrate noise analyst" [6], for the interconnect, which can be extracted e.g. with DIVA [27], and for the assembly. It is shown that for the particular layout of this VCO (see Figure 14), which has been mounted on a PCB, substrate noise impacts the VCO via two ways. For low-frequency substrate noise disturbances and low values of the tuning voltage of the variable capacitors (accumulation-mode n-MOS varactors in this case), the dominant entry point is via the ground lines. High-frequency disturbances enter the VCO mainly via the parasitic capacitance of the inductors in the LC tank.

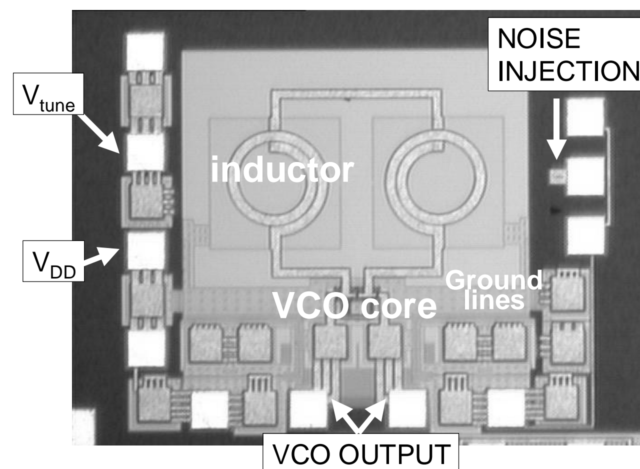

Figure 14: microphotograph of the 3.5 GHz VCO of Figure 3.

The correspondence between measurements and calculations with the model (see Figure 15) is quite good over a broad frequency range of the substrate noise disturbance and the tuning voltage of the varactors. This shows that modeling of substrate noise impact is feasible, although the different steps in the modeling approach (generation of the model of the substrate, interconnect, coupling of these models, generation of the package model) are not yet integrated.

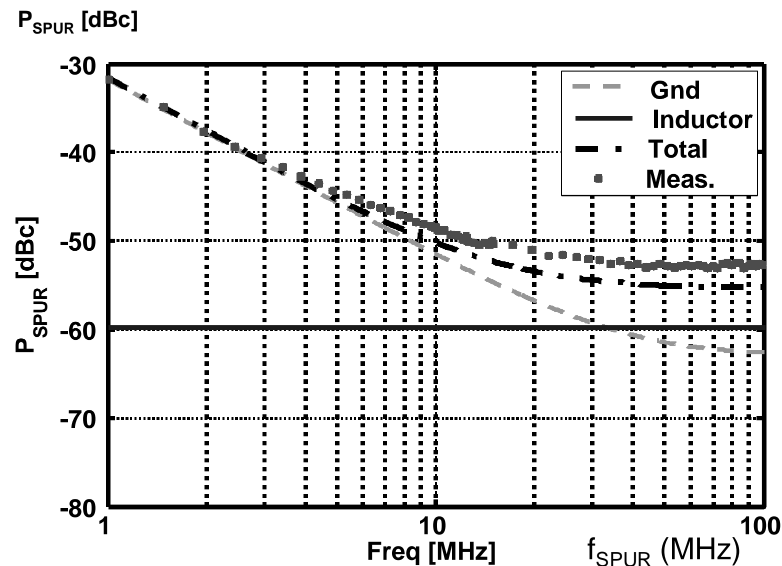

Figure 15: power of the spurious components in the VCO from Figure 3, which oscillates at a frequency f_o= 3.5 GHz. These components result from frequency modulation by a disturbing signal at frequency f_{SPUR} that is injected in the substrate. They occur at $f_o \pm f_{SPUR}$. The tuning voltage of the varactors is 1 Volt. The substrate disturbance enters the VCO via the ground lines (dashed line) and via the parasitic capacitance underneath the inductors (solid line). The power of the spurs is normalized to the power of the carrier of the VCO.

Being able to predict the impact of substrate noise on analog/RF circuits, the next step is to develop design strategies to lower the impact of substrate noise.

6. CONCLUSIONS

Successful integration of analog and digital circuits on one chip can lead to advantages in economics and form factor. However, putting both types of circuits together on a chip introduces an important route for crosstalk from digital to analog , namely the common substrate. This crosstalk, which we call substrate noise coupling, can seriously harm the analog circuits: comparators in A/D converters can take wrong decisions, RF VCOs can be FM modulated by substrate noise, etc. To master the problem, one should be able to predict the substrate noise during design time. The next step is to develop techniques to reduce this coupling. These techniques can only be validated if substrate noise can be predicted with a reasonable accuracy in a reasonable time.

Since the substrate noise coupling is a complicated problem, it is best split into three different parts: generation in the digital domain, propagation through the substrate and impact on the analog/RF circuits. To predict the propagation aspect, both academic and commercial tools are available. To predict the digital noise generation, macromodeling strategies are required, since the problem of noise generation by thousands or millions of gates is too complex to face at the circuit level. Gate-level macromodeling techniques with an acceptable accuracy compared to measurements have been demonstrated on digital circuits of reasonable size, but not yet on multi-million gate designs. Nevertheless, research results on noise generation prediction are sufficiently mature to allow for an assessment of digital low-noise design techniques. Such techniques can reduce the generation of noise with about on order of magnitude.

The prediction of impact of substrate noise is much more complicated as many low-level details need to be taken into account and many entry points of substrate noise into a circuit exist. Careful modeling on specific circuits with a good

accuracy has already been reported, but this modeling is still rather circuit specific. At this moment, this modeling requires the combination of circuit insights, measurements and modeling of the substrate, layout details (interconnect, coupling of the substrate to the parasitics), package and assembly modeling, … A formalization of this modeling work is required to enable prediction of impact. If substrate noise impact can be modeled accurately in a short time, then design techniques for low substrate noise impact can be developed, instead of a rather blind application of different techniques (differential design, use of guard rings, …) as we see today. Only then analog and digital circuits can be put together on a chip without having to resort to conservative designs or without extra design iterations caused by substrate noise coupling. An obvious next step is one integrated approach that operates on a complete mixed-signal design for the calculation of the substrate noise generated in the digital domain and the impact of that noise onto the analog/RF circuits on the same chip.

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