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Lithography Beyond 32nm – A Role for Imprint?

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Abstract

Imprint lithography has been used since the application of the Chinese wax seal to authenticate official documents. In the past century the resolution of the technology has been driven through commercial applications such as vinyl records, CDs and more recently by high definition DVDs. In the past decade, high resolution imprinting has extended the resolution down to sub 10nm features and this fact, coupled with the low cost of the tool, make it attractive as an alternative to other lithographic technologies.

More recently the evolution of imprint lithography from thermal imprinting to UV cured materials, has allowed the technology to operate at room temperature (allowing tight overlay) and low material viscosities (important for high throughput), opening up the potential for CMOS applications. This paper will discuss recent progress in align/overlay, throughput, defect density, materials and the availability of sub 20nm templates, along with tool developments, that make the technology a viable option for advanced CMOS beyond 32nm HP design nodes.

In addition, imprint lithography is being developed for other large electronic markets such as bit patterned media (BPM) for disk drives, and photonic crystals to increase the brightness and efficiency of LEDs used for solid sate lighting, both of which applications are likely to go into production ahead of sub 32nm CMOS. Since overlay requirements are significantly less, whole wafer (as opposed to step and repeat) imprinting is used for these applications, and the presentation will discuss the synergies with CMOS imprint technology.

Key words: Imprints lithography, photolithography, bit patterned media, photonic crystals,

1. Introduction

Despite the remarkable progress made in the past decade in extending optical lithography to deep sub-wavelength imaging, the limit for the technology seems to be fast approaching. At 22nm half pitch design rules, neither very high NA tools (NA 1.6), nor techniques such as double patterning, are likely to be sufficient. The extension of photon based systems to EUV remains very challenging, and this has opened up the opportunity for imprint lithography as a very viable NGL alternative.

Small feature imprint lithography has existed for several years.[1-7] The original technique involved the use of a patterned template which is impressed onto a thermo plastic material and, with the combination of heat and pressure, the pattern in the template was transferred to the substrate.[2] Compact disks were one of the early applications for the technology. Recently the technique has been significantly improved with the development of Step and Flash Imprint Lithography (S-FIL™).[1] This technique was invented by Professors Grant Willson and SV Sreenivasan at the University of Texas, and involves deposition of a low viscosity monomer on the substrate, lowering a template into the fluid which then flows into the patterns of the template. Following this fill step, the monomer is exposed to UV light to cross-link it and convert it into a solid, and the template is removed leaving the solid pattern on the substrate.[1,3] The advantages of this development (low pressure imprinting, low viscosity template filling and room temperature operation) make it uniquely capable for CMOS applications. Although this paper, and this conference, are largely focused on CMOS, it is worth noting that imprint technology can also be used in a wide variety of other advanced applications, many of which are only commercially viable given the availability of low cost (sub $2M) tools capable of delivering sub 50nm features. These applications include the use of photonic bandgap crystals to

enhance LED efficiency and brightness, patterned media for disk drives, polarizers for projection optical engines and a wide variety of other electronic and photonic devices. For most of these applications the capital cost of 193nm immersion lithography is commercially untenable, even assuming that the required resolution limits could be reached.

The purpose of this paper is to describe the recent advances in imprint lithography with particular reference to its application for silicon integrated circuits.

2. Imprint Technology for CMOS Applications

The S-FIL process is shown schematically in Figure 1. The process starts with a template made from a standard 6025 photomask blank, with the pattern etched into the glass using the same technology that is used for phase shift masks. An array of pico-liter sized drops of a low viscosity monomer, are spread across the field being imprinted and the template lowered onto the drops. When the surface tension of the liquid has been broken, capillary action draws the fluid into the template features. Once filling is complete, ultraviolet light, passing through the glass template, is used to cross link the monomer and convert it to a solid. The template can then be withdrawn and the process repeated on the next field.

The use of a low viscosity liquid has several advantages over spin-on films. Firstly, the lower viscosity of the liquid means that material movement and filling of the template are faster, particularly since the drop pattern density can be matched to the pattern density on the template. Secondly the process is intrinsically lower pressure – in fact controlled by capillary action, which also assures that the fluid does not spread outside of the template field. Finally, the use of the "drop on demand" technique prevents the requirement that spin coated wafers be passed into the tool – avoiding the problems of materials evaporation, particle collection on "wet" wafers and the need for a linked track. Since the pattern is "fixed" by UV light, the whole process can be completed at a controlled temperature allowing tight overlay between levels.

Molecular Imprints has commercialized the S-FIL technology, offering a CMOS compatible imprint tool – the Imprio-250™ - which has been designed to take advantage of this type of imprint lithography, and offers the capability of mix and match with 193nm optical lithography with a 26mmx33mm field size, alignment/overlay and magnification control, automated imprint and FOUP to FOUP wafer handling. A photograph of the Imprio-250 is shown in Figure 2.

3. The Advantages and Challenges for Imprint Lithography

Imprint lithography has a number of distinct advantages over photolithography when used for CMOS applications. These include:

(i) Lithographic capability

The imprint process appears to perfectly replicate the template. In consequence the template controls the resolution, line edge roughness and CD control of the imprinted pattern. Since the template has to be only written once, great care can be taken to assure its fidelity. Resolution limits appear to be less than 5nm. An example of research work from the University of Illinois [7] is shown in Figure 3, where a carbon nano-tube based template was replicated – if not perfectly. Since the monomer is of low molecular weight and is physically constrained by the template during solidification, there are none of the resolution/LER issues of molecular size, acid diffusion or areal image that are present in optical lithography. Other data/examples of lithographic quality are shown in Figures 10,12 & 13 and are discussed later in the text.

(ii) No OPC/RET/MEEF or design rule restrictions

Since the template is faithfully replicated by the imprint process – topics such as OPC and MEEF have no meaning in imprint lithography. While manufacturing a 1x template does present some additional challenges – it provides the device designer with complete freedom to design circuits without any lithography based design rules, freeing the designer from optical modeling artifacts. It is truly a "what you see is what you get" technology.

(iii) Lower capital cost

Since imprint tools lack the very complex lens and mirror systems inherent in photon based technologies, nor the need for a linked track, nor the requirement for vacuum and complex sources in EUV, the cost of the tools are significantly less than their competition. In addition, since they are largely mechanical tools, the build times are markedly less.

(iv) 3D printing

Since multi-level or curved features can be built into the templates, the technology has the capability for three-dimensional printing. This has the potential to extend the technology well beyond simple resist and etch capability and into the realm of single step imprinting of dual damascene structures (multilevel features) or direct imprinting of micro-lenses for CMOS imagining devices (curved features). These applications will be discussed later in the paper.

However, as might be expected, these advantages also come with a set of companion challenges. Confronting the technical challenges listed below is the topic of the main portion of this text, but they are listed below in summary form and to provide balance to the advantages.

(i) 1x templates – higher resolution, image placement and defect requirements as compared to 4x photomasks
(ii) Defect concerns – near contact printing
(iii) Throughput – in contrast to photolithography that simply requires exposure for each field, imprint requires not only exposure, but also material dispense, template fill, and field by field alignment.
(iv) Overlay – issues of mechanical magnification control

4. Technical Progress in Imprint Lithography for CMOS Applications

4.1 Templates

Imprint lithography uses templates made with commercial photomask materials and processes. This is a significant advantage relative to previous NGL technologies (X-Ray Proximity and Electron Beam Projection) that struggled with membrane based masks, or even EUV that requires new substrates and reflecting metal films. However, the 1X requirement does test resolution related issues – although not as near to the 4X that might come to mind. The advent of OPC features, which will soon be no more than 1.3x the minimum feature size on the wafer [8] are accelerating the resolution of mask ebeam writers. In addition for imprint templates, since the chrome is only being used as an etch mask (no optical opacity requirements), it is possible to use thinner chrome and ebeam resist than is typical to push resolution down to the required 1x. Image placement is also an issue for a 1x technology, but again, the approaching application of double patterning for 193nm immersion is pressing the existing photomask industry to meet very tight image placement specifications, even for nominally 4x photomasks.

Using commercially available VSB mask writers, imprint templates are already being written down to 35nm dimensions, with very high quality, as shown in Figure 4a [9]. For higher resolution applications, imprint templates can be written with variants of ebeam direct write tools,[10] usually Gaussian Beam systems. These tools have unparalleled resolution, and can easily produce templates with dimensions of less than 20nm as shown in Figure 4b [11] providing an imprint resolution capability well beyond that possible with existing optical technologies.

However resolution is not the only issue for ebeam pattern generators, although it is the most compelling one for device/process development engineers pushing down below 30nm. Photomask write times have been rising rapidly in the past few years – victims of the huge data files required for advanced OPC. Templates have certain advantages in this area. Firstly there are no OPC features required, significantly reducing the number of shots required, and secondly, the area to be written is also a lot smaller. In addition, it is possible to "replicate" template patterns. In this process a single die template is made using an ebeam pattern generator, and then an imprint tool, such as the Imprio-250, is used to replicate this die to create a full field template containing multiple die. For a high volume runner, with four die per field and requiring five mask sets, the effective ebeam write acceleration would be a factor of 20 (four die X five mask sets). This technique has been used in the past for whole wafer, non-CMOS, imprint applications, and an example of the efficacy of the replication process is shown in Figure 5. The potential for lowering write times for imprint templates is important since it opens up the potential to use less sensitive ebeam resists to make the templates. This in turn allows templates with superior line edge roughness and higher resolution.

Template inspection and repair is also an issue since printable features are four times smaller than those for photomasks. To date the most sensitive template inspection techniques have used 1x wafer inspection tools. The KLA ES-32 tool has proved to be effective [12] in detecting sub 50nm defects using a die to die approach as shown in Figure 6a. For die to data base results, NGR [13] has been able to detect 20nm defects using its 2100 tool, as shown in Figure 6b. Repair of template defects can either be completed by mechanical removal of excess material [14] using a Rave 650NM tool, or by replacing missing material using a Nowatech MeRiTMG ebeam [15] enhanced deposition system. Examples of repair are shown in Figure 7. In the case of imprinting, the repairs are required to fill or remove material to a particular thickness, in contrast to a particular optical opacity. Small variations away from the nominal required dimensions are acceptable since this would simply mean that the imprinted resist thickness was slightly different from nominal.

4.2 Alignment and Overlay

All imprint tools for CMOS applications must be designed to mix and match with existing 193nm optical lithography tools. This requires a step and repeat tool with a 26mmx33mm field size, alignment marks that fit into 75µm streets, alignment systems with sufficient contrast and show overlay results on top of 193nm printed under-layers.

The Imprio-250 uses a field by field alignment system, originally conceived for use in X-ray proximity printing, an earlier NGL technology.[16] This does not add to the imprint time since the alignment occurs during the time that the fluid is filling the template features. The "in liquid" align has the advantage that the imprint fluid acts both as a vibration damper and also a lubricant to facilitate the small motions required between the template and the substrate during alignment, reducing stiction effects.

Since the template and substrate are in close proximity (<10µm) during the alignment process, it is practical to capture the relative positioning error between two matching alignment marks using a Moiré image based technique[16, 17].The advantage of using a 1st order Moiré image based technique is that it can provide high resolution alignment data using a low NA imaging unit (<0.05) without blocking the UV beam path. The alignment system utilizes multiple imaging units that can capture not only x, y, theta but also magnification errors. Utilizing the gap insensitiveness of the 1st order Moiré,[16, 18] alignment data can be captured throughout the template fill step and corresponding correction motions are accomplished in a

parallel manner. This system has demonstrated better than 1nm sensitivity of the alignment and positioning system. [16, 18]

Magnification correction is achieved by mechanically compressing the template. Positive magnification can be achieved by writing the template 5ppm oversize and releasing the compression. In this way the required +/- 5ppm can be obtained. Since the distortion is this small, well within the elastic regime of the material, it is perfectly reversible. A multi-point forcing mechanism was developed[19] that can induce optimized vectors of correction forces along the periphery of the template. Such an optimized forcing vector for the mag/distortion correction is computed using multiple relative position data between the template and the wafer that are captured using the alignment system described above. When n-points of forcing per template side are utilized, a vector with a 4n-3 controllability, where 3 stands for three constraints, is available. Therefore, a typical alignment for x, y, theta, mag x, mag y and orthogonality can be compensated.

The efficacy of the alignment and magnification control systems were tested using a KLA overlay tool and AIM/Archer alignment marks. A sample set of results [20] are shown in Figure 8 with approximately 20nm 3 sigma overlay measured for 32 fields and 81 points per field. The major sources of the error are thought to be from thermal distortions, placement errors on the template and image field distortions from the 193nm scanner. Further improvements are expected to reduce the overlay errors down to 5nm.

4.3 Throughput

While slower throughputs may be acceptable for early unit process development and device prototyping, it is clear that production needs of 20wph are required almost regardless of cost of ownership. This represents a challenge for imprint, since it is a multi-step process (fill, overlay, cure etc). The required budget to imprint a field at 20 wph is shown in Table 1.

Table 1 – Field by Field Time Budget for 20wph
(100 fields/300mm wafer)

Stage move, fluid dispense time	0.15 seconds
Alignment, template fill time	1.00 seconds
UV cure time	0.15 seconds
Separation time	0.10 seconds
TOTAL	1.40 seconds

The most significant budget item, and the one specific to imprint, is the time required to fill the template. The two key parameters for fast fill are firstly, drop size and placement and secondly, the template contact angle to minimize any trapped air bubbles. In this latter respect, care must be taken to lower the template in a controlled and inclined angle such that the drops coalesce in a wave front that allows the gas between the drops to be swept out rather than trapped between the drops. The size and placement of the drops are carefully controlled to facilitate this. To do this, the drops, with a size of a few pico-liters, are dispensed using a linear array of several hundred inkjet nozzles that sweeps across the 26x33mm field. The density and pattern of the drops are automatically slaved to the GDS-II file used to create the template, such that the density of the drops is optimized to the template pattern to minimize the amount of material movement required to fill the template features. Under optimal conditions fill times as low as 3 seconds have been achieved in the laboratory and further improvements are expected. The viscosity of the imprint fluid is also an issue relative to fill times. Acrylate based materials (see Section 5.1 below) have viscosities in the 5-10cps range, and other materials such as vinyl ethers are closer to 1 cps.

Future tool designs could use two other advantages inherent to imprint to improve the throughput. The ability to imprint larger field sizes could allow future systems to print four 26mmx33mm fields at once. This would place significant additional requirements on the template fabrication and overlay, but quadruple the throughput. In addition, since the cost of the imprint heads is minimal relative to optical lens stacks, multiple heads could be placed on a single stage platform, further increasing throughput, although multiple templates would be needed.

4.4 Defects

There is concern about the defect levels inherent in imprint lithography since it is a near contact technology. However, it is an error to assume that the problem is similar to that of contact printing for the following reasons:

(i) The template never actually touches the substrate. There is always a thin residual film of imprint material between the two surfaces.
(ii) The imprint fluid drops, which have micron height, tend to cushion any impact between the template and particles
(iii) The template is made from fused silica – a hard and robust material.

Significant progress has been made in reducing the defectivity of CMOS imprints. This progress is shown in Figure 9.[21] While still a considerable distance from what is ultimately needed for CMOS production, the progress has been sufficient for early device development activities. A Pareto analysis shows the defects to have three major sources: template defects, imprint specific defects and particles.

Template defects, as supplied by the commercial photomask vendors are, as might be expected, typically less than 1cm-2 as measured on a KLA 576 inspection tool. The template defect level is increased somewhat by the post photomask processing specifically required for templates (dice and polish, mesa preparation) but this does not represent an insuperable problem. The major challenge is to extend the life of the templates prior to their need to be removed from the imprint tool and re-cleaned. The templates do not "wear-out" since the fused silica is not eroded in anyway by contact with the imprint fluid. However, they can, over time, pick-up defects from partially cured monomer, or other contaminants, after several thousand imprints and need to be cleaned. Since the monomer is organic, the cleaning process is a standard oxidative clean, and early results for in-situ gas phase cleaning show some promise.

Imprint specific defects (micro-bubbles, imprint feature pull-outs etc) have been reduced to ~1cm-2. One important piece of data further suggests that these defects are not very dependent on defect size. A sample of imprinted patterns was tested on a KLA 2132 optical inspection tool with a 200nm pixel size and then retested on a KLA ES32 electron beam tool with a 25nm pixel size. The comparison of the results is shown in Table 2.

Table 2 – 200nm and 25nm Pixel Inspection Results

	KLA 2132 (200nm)	KLA ES32 (25nm)
Template defects	4.8cm-2	6.0cm-2
Particles	2.4cm-2	19.7cm-2
Imprint specific defects	0.0cm-2	0.0cm-2

Although this was an experiment with relatively low inspected area, the lack of defect size dependence for both the template defects and the imprint specific defects is very important since it suggests that the density of these defects is not strongly correlated with size. This is not altogether surprising when considered more deeply. For example micro-bubbles are know to be less stable the smaller they become, and imprint feature pull outs are more dependent on aspect ratio than feature size. The increase in particles as the resolution of the defect detection improved was to be expected. Further work in a cleaner environment, will reduce these numbers.

5. Materials and Processes

For imprint lithography to be successful in CMOS, a complete solution must be available including materials and processes to complement the tool and templates.

5.1 Materials

Successful imprint materials must be formulated with consideration for many requirements and the resulting formulations tend to be very sophisticated [22] to meet the severe yield demands for CMOS. The majority of the work described below is built around an acryate backbone, but vinyl ethers [23] have also been used.

One of the most basic challenges for imprint lithography is how to assure that the material sticks to the substrate and not to the template, even after many thousands of imprints. To reduce the surface energy of the template, a high surface concentration of fluorine is required, but this then restricts the wettability and filling speed, requiring a delicate balance. In addition, any coating on the template is liable to wear and tear, and an in-situ replenishment/repair process is required to keep the defectivity levels down. On the wafer surface, an adhesion promotion film can be used, but needs to be very thin (<2nm) and must be formulated to assure adhesion to multiple surface materials and also with a mind to wettability.

The cross linked material has to be drawn out of the template features during separation. This mandates a material with adequate mechanical strength, toughness and Young's Modulus to maximize the aspect ratio that can be used and yet completely prevent the possibility of a feature being left in the template. Adding polar components helps with these properties but excessive amounts increases the surface tension and reduces the fill speed. The etch resistance must be equivalent to the photoresists. The material must be formulated to be sensitive to UV radiation to assure fast curing, which means attention must be paid to the photoiniators, the wavelength of the exposing light and the prevention of oxygen inhibition.

Viscosity must be controlled. Low viscosities (<5cps) assist faster feature filling,[24] but higher viscosities (10-20cps) tend to be more favorable for ink-jet dispense into pico-liter drops. Lower viscosity materials tend to have high vapor pressures and evaporation rates which need to be minimized or compensated for.

Finally the purity of the material must meet the stringent CMOS requirements of <10ppb (metal ions), not just as formulated, but after passage through the inkjet head assembly.

5.2 Process

For imprint to be successful for CMOS, the tools must not only mix and match with 193nm optical tools, but the imprint materials and processes have to be compatible with the upstream and downstream CMOS processing as well. Most CMOS customers want to place the imprint process into their integrated process without any changes – essentially a drop in replacement for optical lithography.

This has been achieved with the use of the SFIL-O process shown in Figure 1. In this process the organic imprint material has been formulated to be an effective etch mask for silicon based films, and the imprint process tuned to the point where the residual organic layer between the imprinted features is both very thin (~15nm) and very uniform (<5nm 3σ). Since the imprinted features have a typical height of over 50nm (2.5:1 aspect ratio for 22nm HP features), the residual layer can be removed with a quick "de-scum" oxygen etch, prior to etching the hard mask with a fluorine based etch. Typical results for hard mask etching are shown in Figure 10.[25] Excellent resolution, line edge roughness and sidewall angle are routinely achieved. Typical etch ratios between the imprinted material and the underlying hard mask are designed to mimic 193nm photoresists, so that the etching processes can be very similar.

An alternative process called SFIL-R [26] has been developed to provide a positive image of the template on the substrate (as opposed to the negative working SFIL-O process). In this case, following imprinting, a silicon containing film is spun on top of the imprinted features, effectively planarizing the surface. A blanket etch back of the silicon film is made until the imprinted organic features are exposed. At this point the etch chemistry is changed to an oxidative etch which then removes the underlying imprinted features, but leaves the silicon containing material between them intact to act as an etch mask. The SFIL-R process has the advantage of being less sensitive to surface topography on the substrate.

Imprinting has a unique advantage over photolithography, in that one can make multilevel template features. There has been growing interest in the use of multi-level template imprinting to define both levels of a dual damascene pattern with a single step.[27] This can be done in one of two ways. In the first case, a deposited low-k film is patterned with a double level template to pattern both the via and channel features with an imprinted resist. This resist pattern is then etched down to replicate the pattern in the low-k material. This requires that the resist and low-k film etch at the same rate, but surprisingly good results have been achieved.[28] Given the large number of metal levels on advanced logic devices, this offers the potential for significant reduction in cost, and at feature sizes that may be more compatible with 1x template technology. An even greater cost reduction can be achieved, if the low-k material is directly imprinted in one step. This presents many challenges for the material – which must now not only be a viable imprint material but also a viable low-k material as well. However, significant progress has been made in this area, both in terms of material [29,30] and process [29] as shown in Figure 11.

6. Application of Imprint to CMOS

As mentioned at the start of this paper, the most likely production entry point for imprint in CMOS will be at or below the 32nm half pitch node. While the production ramp date for these technology nodes will be out into the next decade, R&D engineers are beginning to require sub 32nm lithography for unit process development (UPD) and device prototyping. This is an excellent application for imprint lithography since sub 32n resolution is easily obtained, the SFIL-O process is fully compatible with existing hard mask etch processes, and the absence of liquid development means that pattern collapse is not an issue. Examples of CMOS UPD patterns are shown in Figure 10. [25]

Further extensions to device prototyping require capability for overlay in addition to resolution. For example, IBM recently announced results [31] on device designs that require densities down to 10nm HP for economic feasibility. Progress with imprint lithography has allowed device structures to begin approaching these dimensions as shown in Figure 12. [32] The 27nm silicon fin structures, built on an SOI substrate, were patterned using SFIL-O imprint lithography, followed by plasma etching with a SiN hardmask. The etched cross sections illustrated in Figure 12, show excellent line edge roughness, CD control and sidewall angles for the etched silicon fins.

Unlike other CMOS NGL technologies, imprint lithography is also applicable to other markets which have similar resolution demands as CMOS, but are likely to go into volume production at an earlier date. One example [33] is bit patterned media (BPM) for hard disk drives. This technology, expected to ramp at the end of this decade, is required since magnetic confinement of the domain is inadequate below 20nm (>500Gb/sq inch density), and beyond this requires the magnetic domains to be individually etched into the magnetic film on the disk. An example is shown in Figure 13. [34] Imprint is the preferred solution for this application given the lower cost and ability to print larger fields (up to 3.5” disks) when compared to photolithography. With over a billion disk drives produced each year, this market alone will be hundreds of tools. The early application to BPM at 20nm will help develop the commercial infrastructure for templates, materials and process technology.

A second non-CMOS market is patterning high brightness LEDs with photonic crystals. These structures look like arrays of contact holes on the surface of the LED and serve to increase both the brightness and the efficiency of the LED. [35] The feature sizes need to be less than the wavelength of the LED emission, and the minimum hole spacing can be significantly less than 100nm. Given the poor surface flatness, and 3” dimensions, of the GaN substrates used for these devices, optical lithography is difficult to use for these dimensions, and imprint lithography is the preferred solution. Photonic crystal enhanced LEDs are beginning to appear in commercial [36] quantities and with broad markets such as back lit flat panel displays, architectural lighting and automotive headlights, this application will also require large numbers of imprint tools over the next five years.

Both the BPM and LED can tolerate lower overlay than CMOS (1-3μm) and the lowest cost of ownership comes from printing the whole substrate at once. Molecular Imprints has developed a companion tool [37] to the I-250, the I-1100 shown in Figure 14, to handle whole wafer imprinting. Like the I-250, the I-1100 is a

fully automated, cassette to cassette manufacturing tool, but uses a thinner, compliant template to allow for the greater non-flatness of the non-silicon wafers.

7. Summary

Imprint lithography has made remarkable improvements over the past five years. The advent of drop on demand, step and flash technology has resulted in significant improvements in overlay, defect density and throughput, such that this technology is now a very viable contender for CMOS NGL. Concurrent improvements in template fabrication, materials and process mean that the technology can be used as a drop in replacement for photolithography but at much higher resolutions and lower cost than competing technologies such as EUV.

8. Acknowledgements

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Figures

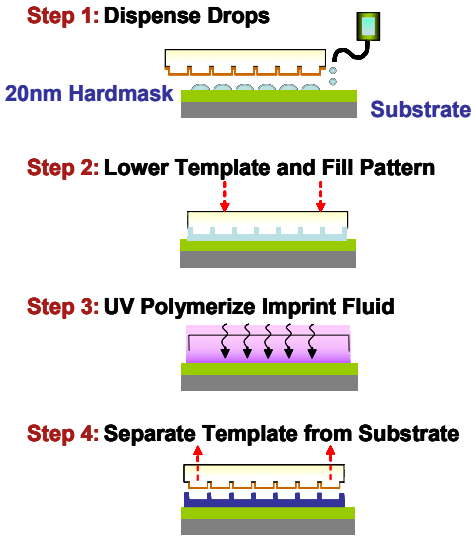

Figure 1. Schematic of the SFIL-O process

Figure 2 Imprio-250 tool for CMOS

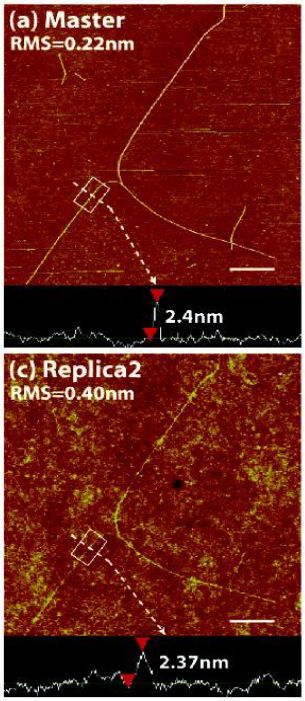

Figure 3 UV cured imprints showing sub 5nm resolution. Top micrograph is the template, lower micrograph the imprinted image. From ref 7.

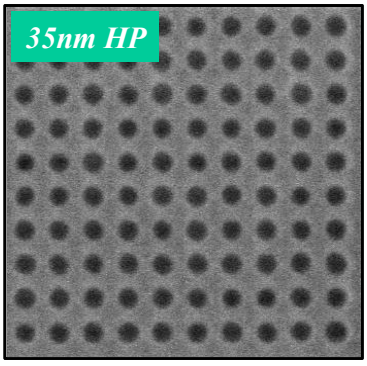

Figure 4a

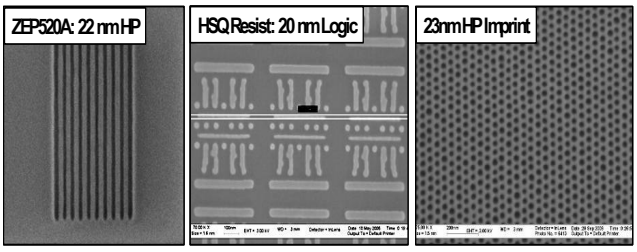

Figure 4 b

Figure 4 showing 1x template patterns.
Top micrograph from VSB pattern generators
Lower micrographs from Gaussian Beam tools
From ref 9 and 11

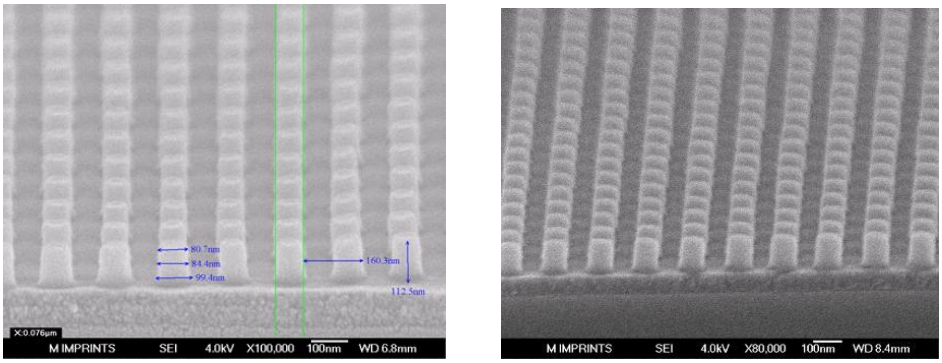

Figure 5: Template replication results. Left hand micrograph shows imprinted features from the ebeam master template, the right hand micrograph shows imprinted features from the replicated template

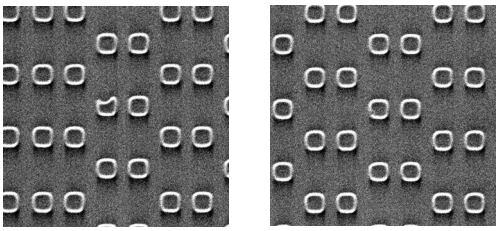

Figure 6a

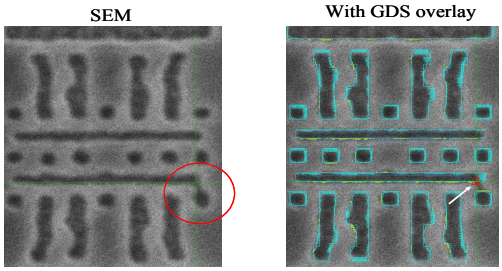

Figure 6b

Figure 6: Template defect inspection results.
Fig 6a showing ES-32 inspection down to sub 30nm resolution (from ref 12) and Fig 6b showing die to data base results at 20nm (from ref 13)

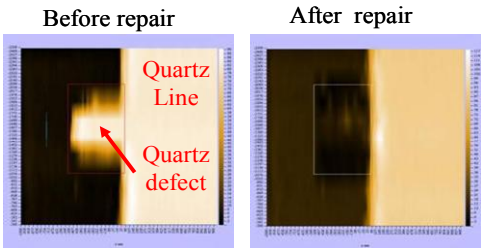

Figure 7a

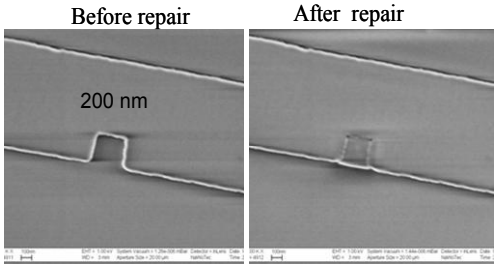

Figure 7b

Figure 7: Template defect repair results
Fig 7a showing mechanical removal of defect (from ref 14) and Fig 7b showing repair of a missing defect using ebeam enhanced deposition (from ref 15)

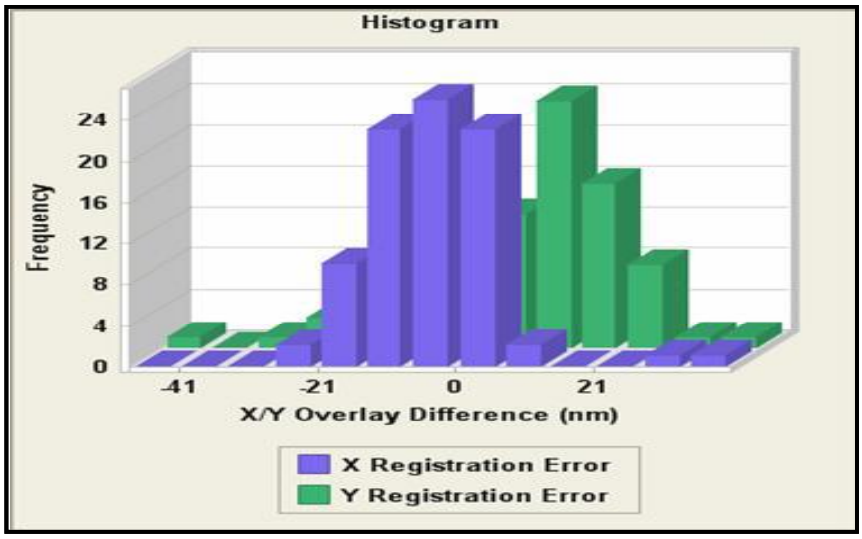

Figure 8: Overlay data from imprint patterns over 193nm optically exposed underlayers. 32 fields per wafer and 81 locations per field (from ref 20)

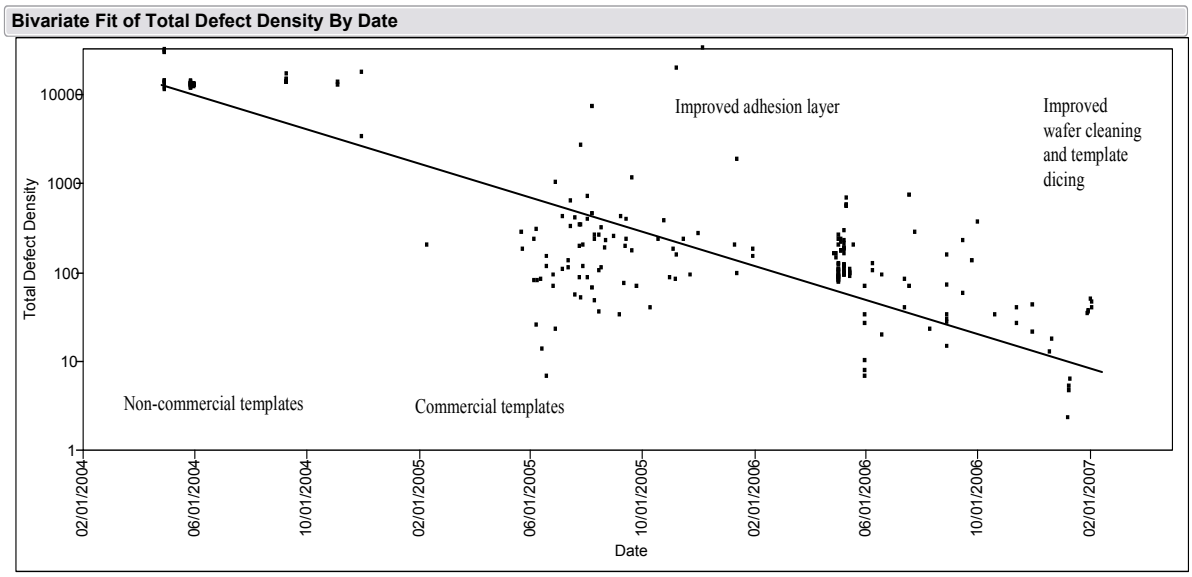

Figure 9: Defect improvement over time for SFIL.(from ref 21)

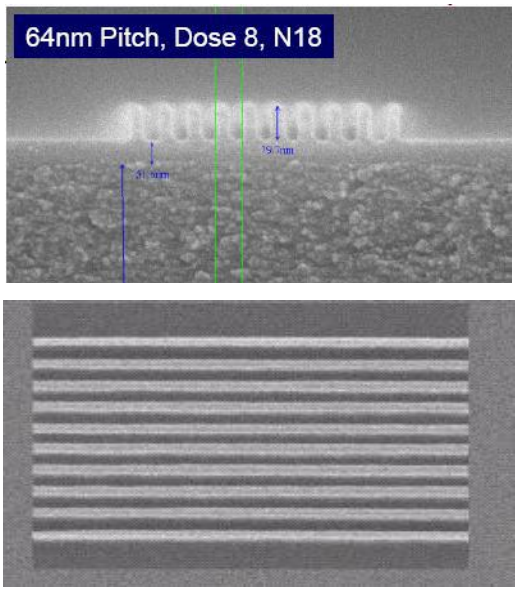

Figure 10: Cross section and top view images of 32nm half pitch imprinted features showing excellent wall angle and line edge roughness (from ref 25, with a template made by DNP)

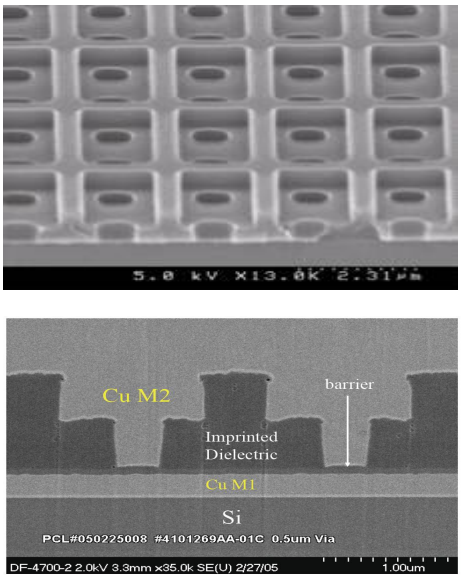

Figure 11: Imprinted low-k dual damascene results showing the top view of the imprinted low-k dielectric and a cross section after barrier metal and copper fill (from ref 29)

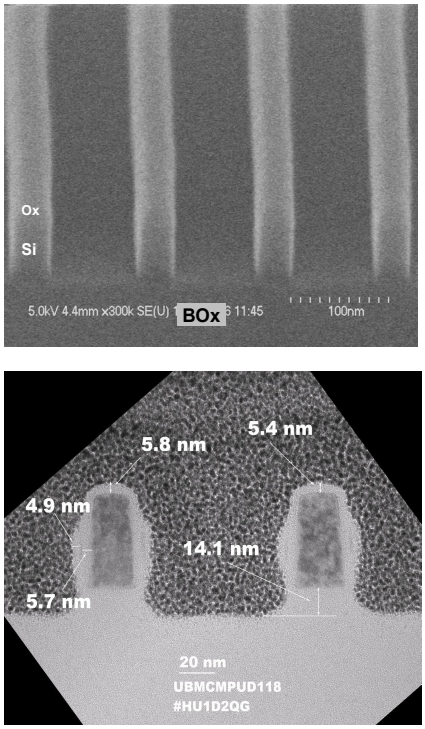

Figure 12: Cross section views of experimental device from IBM (ref 32). Top micrograph, 27nm silicon fins, imprinted and etched; lower micrograph, cross section of the device

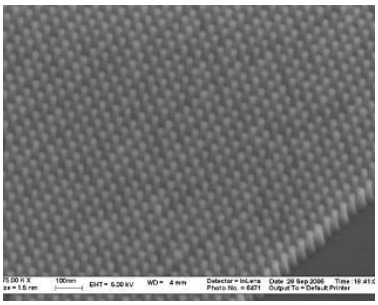

Figure 13: Sub 30nm half pitch patterns for BPM (from ref 34)

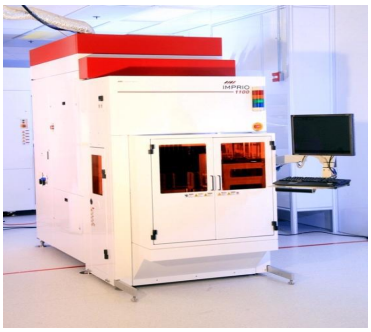

Figure 14: Imprio-1100Whole wafer, conformal imprinter for LED, optical component and BPM applications