How Will Photonic Integrated Circuit Technology Develop?

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ABSTRACT

This paper explores issues associated with Photonic Integrated Circuit (PIC) research and development – with an overall goal of initiating a discussion of how PIC technology should develop and eventually be deployed with high impact. Significant research and development programs have focused on PICs for routing and switching, and computer interconnects. Most recently, the application domain of PICs has diversified greatly, and now includes analog signal processing, remote sensing, biological and chemical sensing, neural interfacing, and solar cells. A key feature of PIC technology growth has been the exploitation of high-density fabrication and packaging technology originally developed for the Silicon IC industry. PIC foundry services are emerging – and there has been a natural attempt to ascribe a "Moore's Law" to PIC scaling. Analogies to Silicon electronic scaling, however, should be used with caution. PIC complexity scaling may be driven more by the ability to access the degrees-of-freedom offered by PIC-based optical domain signal processing, rather than increasing device count. Specific examples of PIC research in chip-scale computer interconnects and integrated micro-concentrators for solar cells are highlighted.

Keywords: Optical Interconnects, High Performance Computing, Integrated Optics, MQW Modulators, Solar Cells.

1. POTENTIAL PHOTONIC INTEGRATED CIRCUIT APPLICATION DOMAIN

Much research and development has been, and is currently, focused on applying photonic integrated circuits (PICs) to chip-scale digital optical interconnects (OI) for high-density, high-throughput, computer communications [1-8] and networking [9]. In OI there is a specific goal of overcoming the performance limits of high-density metal interconnects and there has been an emphasis on developing monolithically integrated Silicon Photonic platforms to exploit the fabrication precision and device densities associated with Silicon ICs, as well as the potential for tight integration with Silicon electronic circuits. However, as evidenced by recent initiatives at the Defense Advanced Research Projects Agency (DARPA) and other sponsoring agencies, the PIC application domain may expand well beyond OI. The diverse application domain being considered for PICs now ranges from analog signal processing, to routing, to remote sensing, to biological sensing, to solar cells.

This widening application domain will likely entail exploitation of a diverse set of technology platforms to match to the particular demands of processing and interfacing for each application. One can imagine a set of application-specific platforms optimized to address the particular performance requirements. One common challenge for all applications will center on engineering the interface between the PIC and optical energy that it exploits – be it for sensing, signal processing, computing, actuation, or energy transduction. Given this focus on optimizing the interface, it is anticipated that PICs will often involve hybrid integration and packaging of differing technologies. Such efforts should be able to leverage the advances made in Silicon IC packaging.

Figure 1 depicts the expanding application domain of PIC technology as a pie-shaped chart. Four major areas of application – computation, sensing, actuation, and energy generation are presented as major pie sections (slices), corresponding to areas of interest being explored by the Defense Advanced Research Projects Agency (DARPA) and other government sponsoring agencies. A pyramidal "base" at the bottom of the chart is reserved for basic research projects, which, as depicted by the green arrows, can serve as foundational work before development in the four major areas.

Sub-sections of the pie chart (labeled with blue background) depict specific areas of focus within the four areas. These areas and sub-sections are not meant to be exhaustive – in fact it is possible that as PIC technology matures, other important applications will emerge. Some specific current and recent PIC R&D programs at DARPA are displayed in their appropriate segments of Figure 1 (The depicted set of programs is meant to be exemplary only and is not

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comprehensive.). The specific challenges and PIC technologies developed for these programs can be found in numerous sources and publications in the literature. Here I simply put them in the context of an overall PIC R&D space.

The pie-chart representation is a useful construct to visualize how future R&D efforts may develop. New R&D efforts may appear within each subsection of Figure 1, increasing the number of "slices in the pie." For example, under the actuation sub-section, a "neuro-photonic" program may develop based on preliminary research done in this area as part of the DARPA *CIPHER* program or related efforts to exploit new ideas in photonic actuation and sensing interactions with living neurons – which may hold promise for the prosthetic field and other medical applications. Other PIC-based actuation concepts, such as those based on opto-fluidics, may emerge, thus proving a path to expanding that section of the pie chart. In the sensing section, PIC-based bio-sensing R&D may also expand – also based on *CIPHER*-funded or other basic research area, where much activity is taking place to exploit chip-sale bio-assays for diagnostic and medical research purposes. Fabrication and circuit technologies needed for precise phase control developed in the *PhASER*, Si-*PhASER*, *SWEEPER,* and other non-DARPA efforts, may be exploited in new application areas within the computation section. For example, such capability could bring about new concepts in energy efficient and ultra-high-throughput computational elements and architectures. The newest area exploiting PIC technology is in the energy area – where the integration of micro-optics, pixilated photo-voltaic (PV) cells, and possibly micro-actuated tracking mechanisms, represent an entirely new PIC application – with completely different challenges than the laser-based PIC notions in the other sections of the chart.

Imagining the chart of Figure 1 expanding in the radial dimension – as the sophistication and functionality of PIC platform technology expands – provides a visualization of how the PIC application domain may expand. Given the diversity of performance challenges, the radial expansion along the spokes of the charts are not likely to be uniform, as overviewed in the following section on scaling. Sections 3 and 4 below discuss the potential performance pay-offs of applying PICs to two radically different applications: Computer OI and PV solar cells.

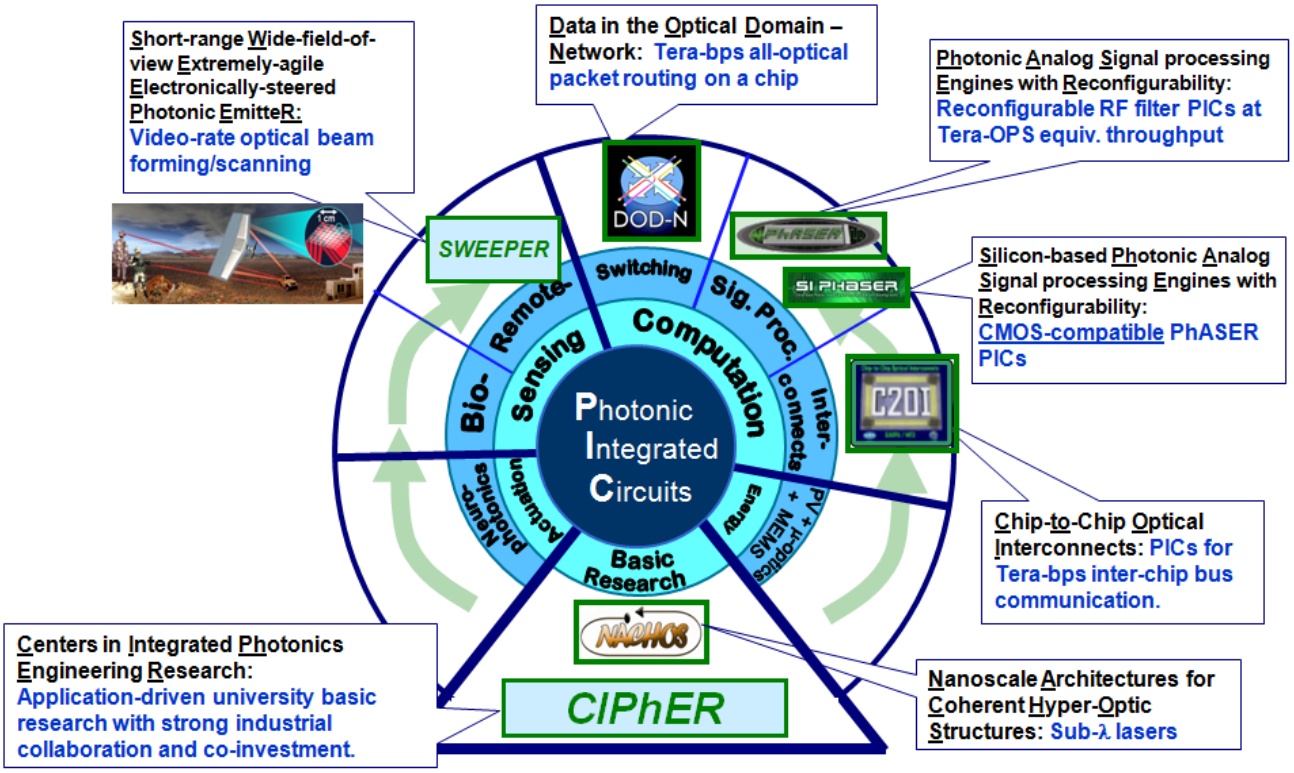

Figure 1. Pictorial model for PIC R&D development across an expanding application domain – As PIC technology becomes more sophisticated in terms of functionality; we can imagine the pie expanding in number of slices and size. In this notional model, the pie sits atop a platform of basic research. Current and recent DARPA-funded programs are shown as examples of the widening variety of PIC applications.

2. HOW WILL PIC TECHNOLOGY SCALE?

With the familiarity and impact of Moore's Law economic and performance scaling [10] – which has driven electronic IC development for 5 decades – it is reasonable to ask whether PICs will benefit from similar exponential scaling as the technology platforms develop and are inserted into the application domain. Certainly PIC technology development will continue to exploit S-O-A lithographic technology developed for electronic ICs. However, although sub-wavelength structures are, and will continue, pushing PIC technology scaling, it likely that scaling will be not dominated by device density (as in Moore's Law), but rather by the tremendous degrees-of-freedom scaling offered by integrated photonic technology based on the large bandwidth available in optical channels and the various methods available to exploit that bandwidth. Long-haul fiber optic technology has maximally exploited the photonic channel capacity by tapping into bandwidth, wavelength, phase, and polarization diversity of photonic signaling. Similarly, PICs, exploiting precise fabrication and phase control of coherent light will continues to scale in circuit functionality. However, PIC scaling will have the added degrees-of-freedom associated with the spatial dimension to enhance capacity, wherein high density channels and devices dramatically compound the overall degrees-of-freedom afforded to PICs.

Each of the application areas will have specific performance metrics. "Throughput" will be a general performance measure for PICs similar to the operations-per-second (OPS) measure variously used to characterize electronic ICs. However PIC "OPS" will take on application-specific meanings that do not relate directly to the digital IC usage. For example analog signal processing PICs may use a metric based on the product of bandwidth and filter complexity. Remote sensing phased array PIC technology, such being developed in the DARPA *SWEEPER* program, may use the number of resolution spots and scan rate in its definition of OPS. Bio-sensing PICs may want to maximize the number of high-resolution assays per unit of time. What's more, the definition of throughput in the solar energy harvesting arena may be generalized to include metrics such as W/Kg. No matter what the application, some measure of throughput will be important and will inform the performance scaling of application-specific PIC technologies.

Figure 2 is a notional depiction of how PIC scaling may compare with CMOS scaling. Whereas Silicon IC chip complexity and throughput has been directly proportional to transistor density (Figure 2a), PIC technology scaling will likely follow different scaling paths that are dependent on the specific application and PIC technology platforms used. As mentioned above, rather than device density, the degrees-of-freedom, as determined by spatial and spectral bandwidth measures offered by the PIC, will govern scaling. This may provide some measure of exponential scaling similar to Moore's Law, but most likely with distinct differences in time-line and impact. The traditional cycle of "killer app" driven technology scaling, that has been the hallmark of Silicon IC development, will likely not be appropriate for PICs. Rather PIC performance will scale upward based on differing measures of performance throughput and reduced cost with increasing market size.

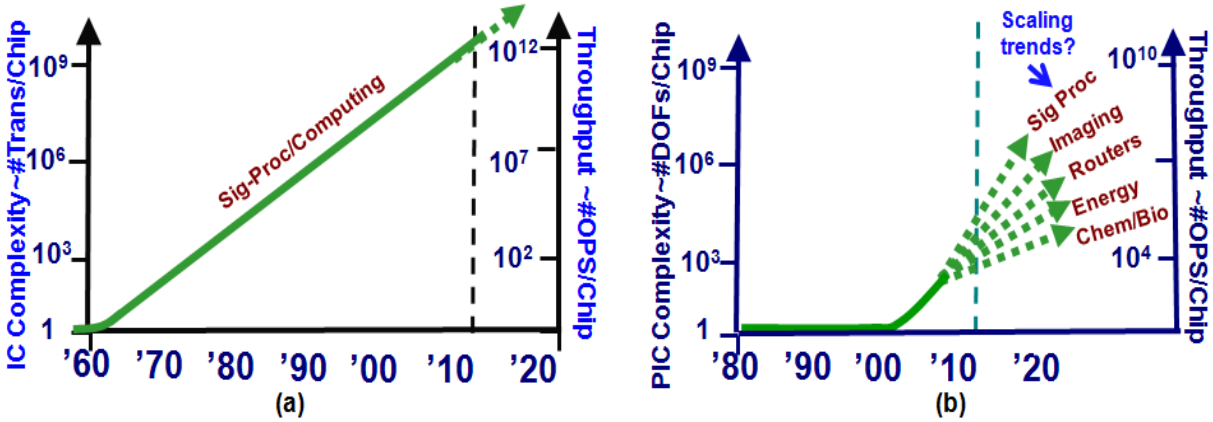

Figure 2. Schematic depiction of Moore's Law scaling for Silicon IC technology (a) as compared to possible scaling for PIC technologies (b). (The dashed lines representing different PIC applications are not predictions, but simply meant only to highlight those different scaling paths will be followed. Unlike with Silicon ICs, PIC complexity will not be determined primarily by node size or device count, but rather by a more generalized "degrees-of-freedom" afforded by operating in the photonic domain, and will vary depending on the application and PIC technology platform used. The notional scaling of PIC technology may still take on an exponential nature (as notionally depicted) for some applications.

3. EXAMPLE: PICS FOR INTEGRATED CHIP-SCALE COMPUTER INTERCONNECTS

Chip-scale OI technology has been under development for over a decade – both at the intra- and inter-chip levels [1-8, 11, 12] – and is now poised to enable high performance computing (HPC) to continue to scale with Moore's Law until the eventual end of CMOS scaling. Achieving this will require chip I/O levels that scale with on-chip processing power [13]. As shown in Figure 3, this will require chip-scale signaling in the ~100's fJ/bit range, which is beyond the capabilities of current metal trace based signaling technology. PIC technology has been projected however to achieve this level of interconnect efficiency, with the densities needed to scale with HPC Silicon chips of the future [14, 15].

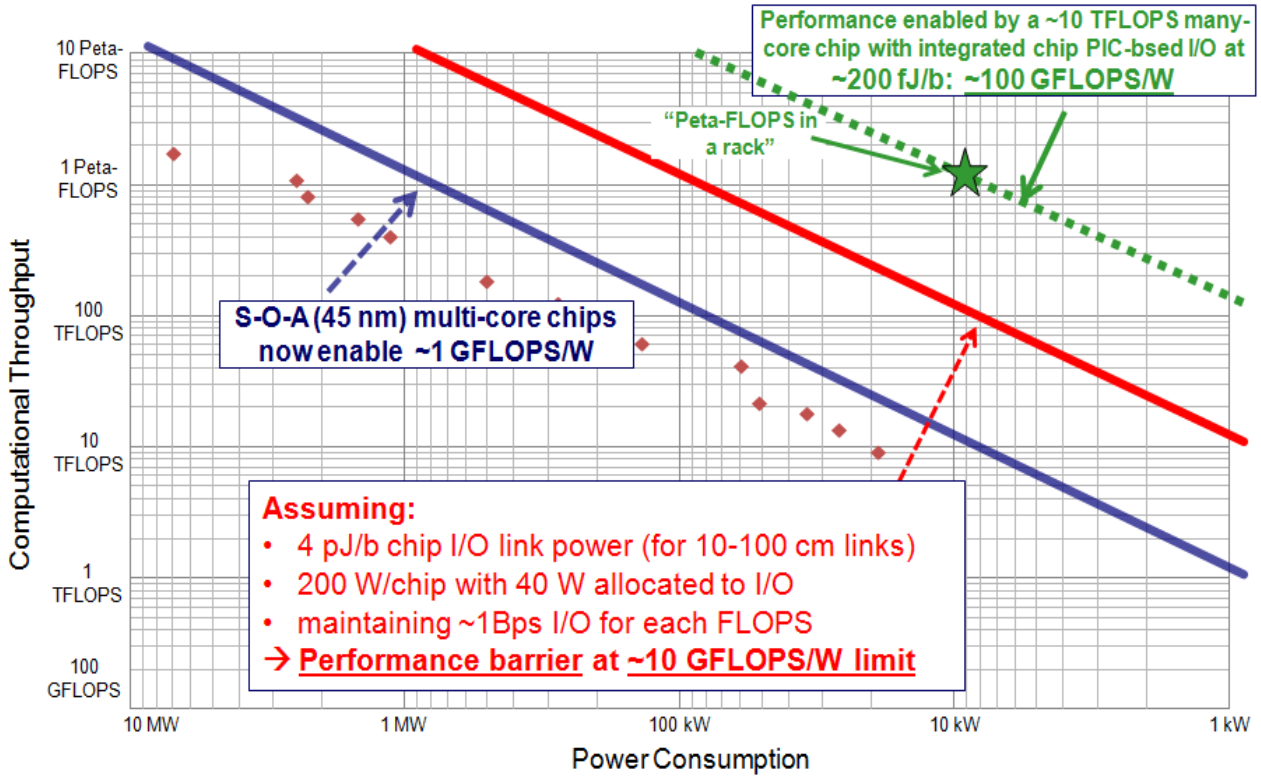

Figure 3. (adapted from [13]). Modern HPC systems maintain roughly constant FLOPS/W performance across several orders-of-magnitude in computational throughput as shown by red diamonds corresponding to systems in the 2010 timeframe. The blue line is a project of state-of-the-art HPC performance. Metal trace-based interconnects presents a barrier to HPC scaling due to their E/b requirements at the inter-chip level (red line). However, with anticipated Moore's Law chip scaling to the 10 TFLOPS level for 200 W chips, if the chip-level interconnect barrier can be breached, HPC performance can potentially scale to ~50 GFLOPS/W performance (dashed green line). At this level, Peta-FLOPS-in-a-rack becomes realizable – and, by extension, Exa-FLOPS performance for large HPC systems will be within reach.

4. EXAMPLE: PICS FOR INTEGRATED SOLAR PHOTOVOLATICS

A new area of opportunity for PIC technology is in solar power energy conversion based on PV. Traditional PV technology advancements rely on improving device performance through better PV materials, device designs, multi-junction implementations, and engineered light trapping. Concentration is also employed to decrease the amount of expensive PV material and improve the performance of the PV cells. Figure 4 shows the trade-off in power density vs. mass density found in conventional commercially-available PV cell technology spanning from the simplest flexible polymer cells to large bulky concentrating PV (CPV).

Cost is the primary driver for commercial power generation. However, some mobile applications are also concerned with reducing the mass of the PV cells – and increasing the output power per unit mass. Exploiting the PIC technology

for solar PV may provide a path to significantly increased W/Kg performance, with small footprint systems, as well as provide reduced cost per Watt due to the economies of scale that will come with mass production of PIC-based solar cells integrated in large arrays with inexpensive pixilated solar concentrators.

One example of such a new PV approach is the Micro-systems Enabled Photovoltaics (MEPV) concept [16, 17] that integrates micro-optical concentrators with pixilated photo-voltaic (PV) cells fabricated with lithographic and packaging technologies to provide cells arrayed across a wide panel area. The goal is to provide the benefits of concentration and multi-band gap performance in a low profile architecture that mimics conventional flat panel PV cells in outer appearance and cost, but provides a significant jump in conversion efficiency and overall power output per unit area. Both lateral [16, 17] and tandem [18, 19] cell configurations are being considered to exploit the benefits of multi-junction performance and concentration at the micro-scale. As with conventional PV cells, various engineered interface and light-trapping notions may be incorporated to enhance performance. The MEPV approach to the integration of micro-optics with the PV sensor at the micro-scale may provide a path to overcoming the observed trade-off in power density and mass density as shown in Figure 4.

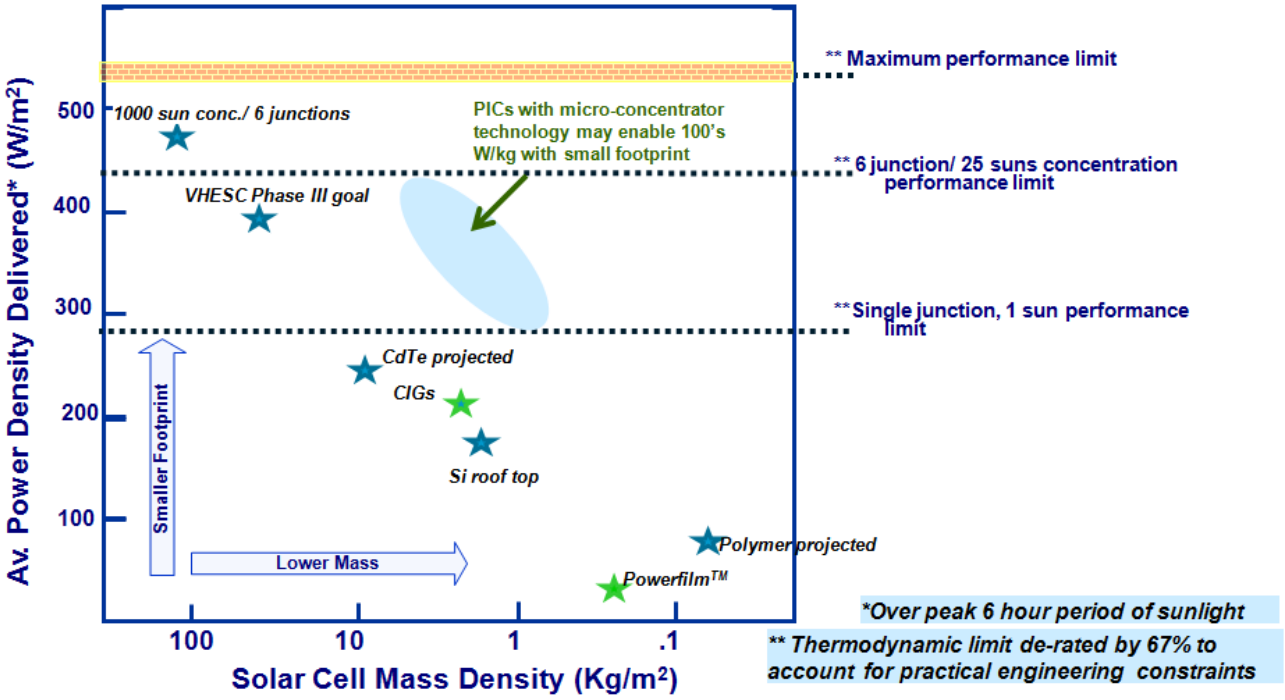

Figure 4. A plot of commercially available solar technology shows a trade-off between power density and mass density. It is envisioned that combining PIC technology and micro-concentration will enable PV performance that achieves unprecedented power-per-mass (blue oval) within a small footprint. The goal is to exploit the economies of scale for mass produced solar PV PICs and micro-optics to enable lower performance per cost than conventional PV panels may achieve.

5. SUMMARY/CONCLUSIONS

The ever-increasing precision of fabrication, circuit functionality, and yield of PIC technology position it to expand into a wide range of applications that extends well beyond digital computer interconnects and networking –including multiple sensing, actuation, and energy harvesting functions. All of these applications will benefit from the degrees of freedom afforded by PIC technology at the "chip-scale." PIC foundry technologies will be required to address the diverse needs of the applications and their PIC technology platforms. Key challenges to mapping PIC technology onto applications will involve overcoming the interfacing challenges between the PIC and the optical signal being processed through or on the PIC. The developments of hybrid PIC integration techniques will therefore be key to addressing these challenges – and enable PICs to have significant impact across a diverse application domain.

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