# A unique new microtechnology facility for Australia

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## ABSTRACT

The **Queensland Microtechnology Facility** is an initiative of the Queensland Government in conjunction with Griffith University. The Queensland Government through its **Smart State Research Facilities Funds (SSRFF)** is providing funds for equipment to equip a purpose built building provided by the University. The focus of the Facility is on the application of **Silicon Carbide on Silicon** semiconductor systems. This is an important feature that enables access to the mature silicon technology at the same time providing access the less mature but very promising SiC technology and its properties. These properties include broad bandgap, thus high voltage and high temperature operations, excellent mobilities, very small leakage currents and high thermal conductivity.

The QMF is unique in that it will encourage state of the art research with a commercial bias. It will be equipped with custom built equipment to meet the goals of the Facility. Already there are projects directed toward the exploitation of Silicon Carbide on Silicon Technology being undertaken. This paper provides some background to the planning process associated with the realisation of the QMF.

## 1. INTRODUCTION

The Queensland Government through its Smart State Initiative have a number of support programs that aid high quality research, the research in turn has the potential of significant financial and other flow on benefits to the state. One such program provides infrastructure support (buildings and equipment) and is know as the **Smart State Research Facilities Funding(SSRFF)** program.

A recent bid for support under the SSRFF program was made to forward the Stored Charge(Qs) Memory work which was the subject of a patent [1] by Dimitrijev and Harrison of the University. The bid was essentially to provide equipment[2] that would be used to populate a purpose built building to exploit the patent and further IP generated around the patent.

The patent refers to silicon carbide(SiC) as a possible material on which the memory technology could be developed. Previously this material (SiC) was used to advance a number of different applications as outlined in figure 1 below [after 3]. These applications make use of the unique properties of SiC such as broad bandgap, which brings with it very low leakage both surface and bulk, high thermal conductivity, silicon dioxide as a dielectric and of course being a semiconductor brings with it the well established simulation regimes which of course silicon enjoys.

Each of the five areas listed in figure 1 are also commented on, these include microstructures, optoelectronic devices, high temperature electronics, rad hard electronics and high power/high frequency devices.

In this paper further justification is provided on the use of SiC as a memory material and what is needed to process the material to make it commercially competitive. As indicated in figure 1 it has significant potential as a non volatile random access memory material. After assembling this information a building blueprint is developed along with an equipment complement that is being put in place to establish this unique facility which because of the State Government/ University commitment is called the **Queensland Microtechnology Facility(QMF)**

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| Applications | Comments |
|---|---|
| Microstructures | This includes X-ray masks and Micro-machined structures such as those for high temperature environments |
| Optoelectronic devices | Substrates for the nitride family of devices, light emitting diodes, UV detectors etc |
| High Temperature electronics | Because of the large band gap almost all devices fall into this category |
| Radiation hard electronics | Nuclear reactor electronics, military systems, deep space electronics. |
| High power/high frequency devices | Good thermal conductivity and improved mobilities and MOSFET structures have seen commercially acceptable devices developed. |
| ***New memory technologies*** | ***Charge retention properties of SiC will be exploited for non volatile random access applications*** |

Figure 1 Applications of Silicon Carbide

## 2. FACILITY FOCUS

The focus for the QMF is on world class research into the applications of the material silicon carbide. This material however has many different poly types that have their own unique properties and stages of technical development. For example the poly types 4 and 6H(Hexagonal) are produced by "step-controlled epitaxy"[4] on a wafer sliced from a boule after sublimation growth. The resulting wafers are of high quality but with limited diameter(<100mm) and thus limited real estate (area). A brief cost comparison for materials in 2003 put silicon at 0.2USD/cm2(200mm wafer) compared to 50USD/cm2 (50mm) for SiC.

Even though SiC material improved dramatically throughout the last years of the last decade it was not until early this decade that major breakthroughs were made in the quality of the interface between the SiC epitaxial layer and the silicon dioxide passivating layer [5]. This improvement resulted in significant reduction of the number of interface traps and importantly a vast improvement in the near surface mobility. This thus provided a very strong platform for the application of SiC to MOSFET type structures including MOSFET [6] high power/high voltage devices. Indeed this fuelled a resurgence in SiC for power and other applications and new research and development laboratories began to re appear around the world. However given the cost data presented above SiC could never compete head on with silicon but is more suited to niche type applications.

At around this time the group at Griffith University that pioneered the improvements in the interface properties also discovered another important property of the improved interface. By forming a simple MOS capacitor structure the charge retention time measured at room temperature was significant and indeed to study the electrical properties of this structure required that non equilibrium conditions be imposed. The results of early experimentation are show in figure 2 which highlights this outcome [5,6].

These results are very interesting in that both 4H and 6H material were studied with the MOS dielectric being formed under different gas growth conditions. In both cases a nitride based gas was used along with dry oxide to form the dielectric and on <100> SiC surfaces. The activation energies for 6H is lower than 4H to be expected because the bandgap of 4H is larger than that of 6H(cf 3.26eV compared to 3.02eV)[ 3]. The charge retention time is gained from a simple discharge curve taken at that temperature, for example at ~300C for 4H SiC(top curve) this time is about 10e4 seconds(2.7 Hours), or at room temperature around 10e10 years, and for 6H SiC, 10e6 years. For non volatile memories a time of ten years at temperatures greater than 100C is usually accepted.

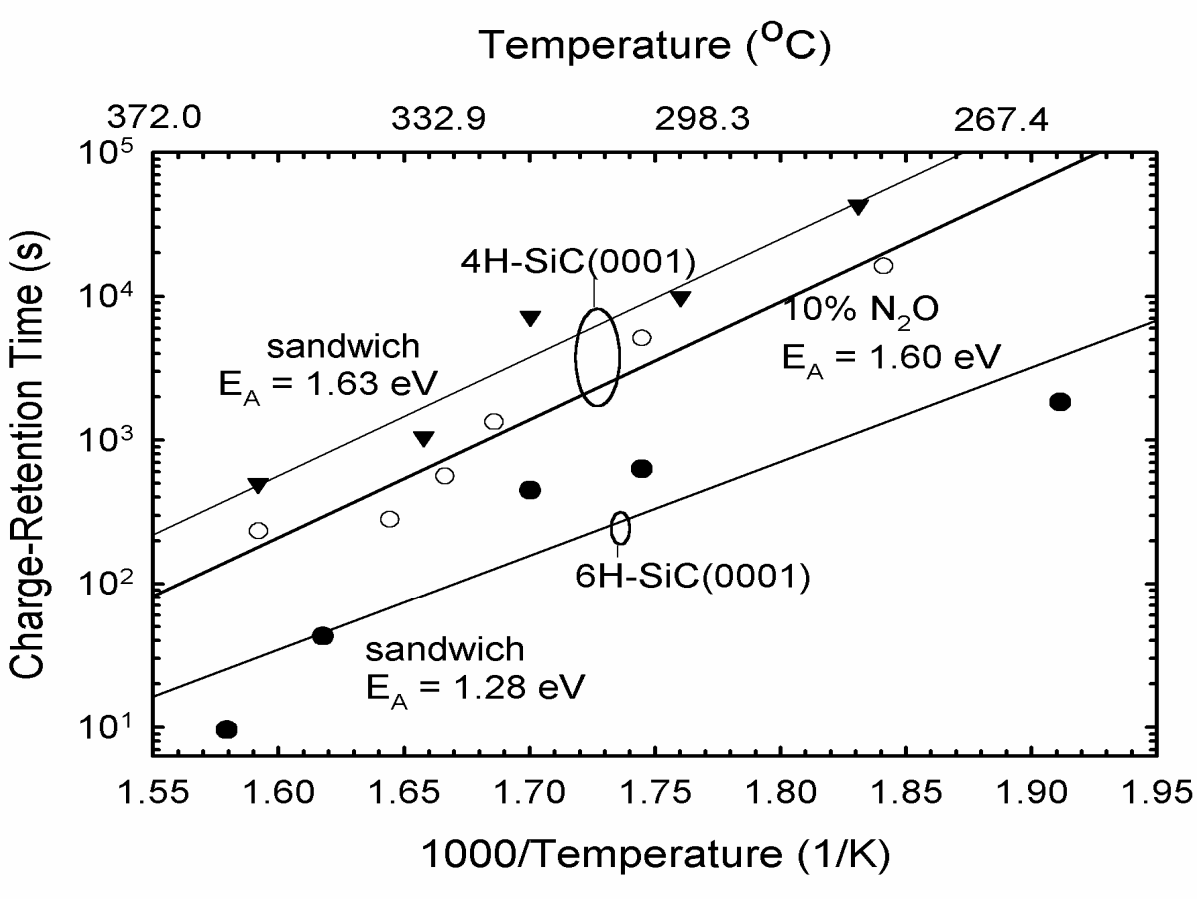


Figure 2 Retention of Non equilibrium Charge in SiC MOS Capacitors

These figures suggest that these materials would be quite suited to non volatile memory applications if a suitable memory cell configuration could be found. If for example silicon technology was followed then the simple DRAM one transistor on capacitor cell would suffice. However if the gate is used to store the charge then the capacitor could be compressed into the transistor and a one transistor cell would be possible [1]. All this is with the background of the deficiencies of 4 and 6 H SiC namely the non competitive commercial nature for many applications.

A further poly type of SiC is the cubic form 3C- SiC, this is a narrower band gap (2.4eV) poly type than 4 or 6H but still well above that of Silicon(1.12eV) and should have respectable charge retention properties. A big draw card of this material is the fact that it can be grown epitaxially on silicon. Thus if front end processing, at temperatures low enough to be compatible with silicon can be achieved than a modified silicon process can be used and the entry cost barriers that other poly types bring can be considerably lowered. Further the final product should also be cost competitive with any existing or new memory technology.[7]

Consider the epitaxial growth of silicon carbide on silicon, because both have cubic crystal structure then epitaxy is possible. However the atomic lattice spacing are quite different and thus the lattice mismatch resulting from the epitaxial growth is quite large(20%) and causes stress problems that result in physical and electrical defects. To grow a layer of silicon carbide on silicon a two stage process is usually adopted viz carbonisation (1) and epitaxy (2). In the carbonisation step the silicon is exposed to a carbon rich environment and a very thin layer of the silicon surface is converted to Silicon Carbide. This thin layer (1) acts as a seed layer for the epitaxial growth of a thicker layer grown in a balanced silicon/carbon gas mixture (2). During this growth phase dopants can be added and multi layer structures formed. To assist with the thermal budget and enable a lower deposition temperature a pressure controlled environment for this second step is usually employed.

Conceptually a single transistor memory cell is outlined in Figure 3 below. A two stage epitaxial process is employed along with etching, oxidation and finally poly gate deposition and delineation. These steps are an addition to any further silicon work that may be added for the access electronics. As long as the carbonisation and epitaxial process are at a low enough temperature and the memory areas do not produce significant stress then the process will enable large memory capacity coupled with sufficient silicon support circuitry to produce a cost effective technology.

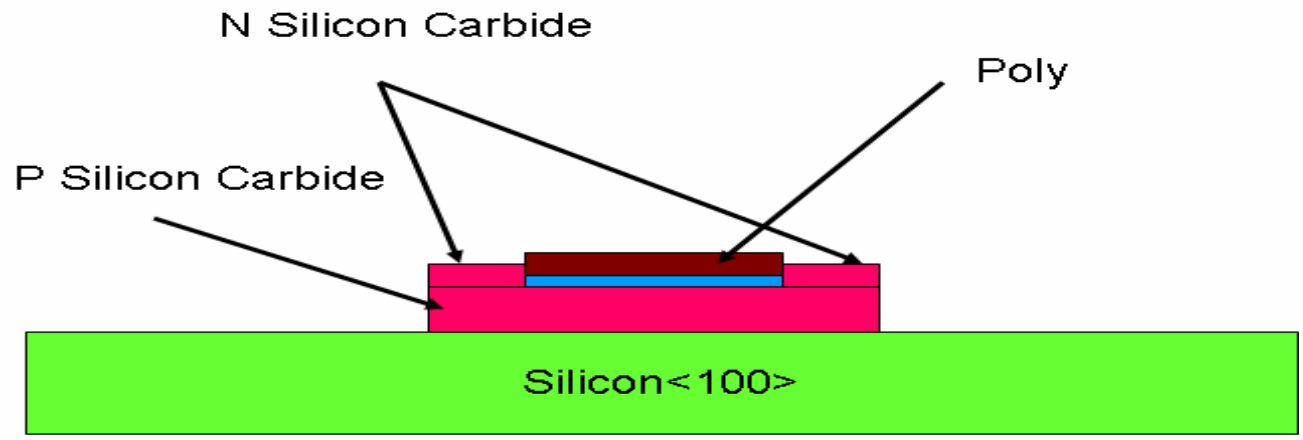


Figure 3 Schematic of single transistor memory cell

3C SiC has not been advanced significantly in the past due to the dominance of the other poly types. The commercial push put behind the larger bandgap materials(4 and 6H) has meant that 3C on Si technology has not advance significantly since the mid nineties. However some activity has transpired with the deposition of 3C SiC on Si for MEMS [ 8]. This has been achieved with technologies completely incompatible with silicon technology (temperatures too high) and thus a process window has yet to be found for this compatibility and thus a major area of research for the QMF.

The QMF then has as its focus the development of SiC on Si compatible technologies mainly for memory applications but if other applications evolve they may be explored.

## 3. SiC ON Si PROPERTIES AND TECHNOLOGIES

Silicon process technology is generally well know and predicted through the semiconductor road map [9]. For 3C SiC technology to become part of this road map requires the integration of the front end SiC with the general silicon processes. Things in silicon technology that are well know are that wafer technology is strongly advancing toward 300mm with minimum feature sizes smaller than 100nm. However for proof of concept that the QMF aims toward, needs front end process conditions that will be scalable in the future but will give confidence of that scalability to be established. For instance we have chosen 150mm wafer diameter as the working material knowing that results obtained on these wafers are scalable to 300mm technology. This diameter was also chosen to be consistent with Peregrine Semiconductor Australia (PSA, Sydney) who will provide some services not being planned initially for the QMF. Minimum feature sizes to predict sub 100nm dimensions operation can also be achieved with micron size feature sizes in the first instance as long as the software simulation packages used to predict smaller dimension operation are robust enough.

| Process Step | 3C-SiC Compatible | Comments | Silicon Compatible |
|---|---|---|---|
| **Doping** | **Common Dopants**<br>N type, Nitrogen(0.053eV),<br>Phosphorus(unavailable)<br>P type, Aluminium(0.271eV)<br>Boron(0.73eV) | | |
| - Thermal Diffusion | No | Requires extreme temperatures | No |
| - Ion Implantation | Yes | Requires high temp implant and anneal | Maybe |
| - Epitaxy | Yes | Requires tight gas conditions | Yes |
| **Oxidation** | | | |
| - Thermal wet and dry | Yes | Good surface passivation and oxides | Yes |
| - CVD | Yes | Untested for quality at this stage | Yes |
| **Etching** | | | |
| - Wet Chemical | No | Almost chemically inert | |
| - Dry | Yes | Must be careful of masking process | Yes |
| **Other depositions** | | | |
| - Nitrides(CVD) | Yes | Similar to silicon | Yes |
| - Metals | Yes | Similar to silicon | Yes |
| - Ohmic contacts | Yes | Reasonable contacts | Yes |
| **Lithography** | | | |
| - Optical reduction<br>Step and repeat | Yes | 3C is transparent yellow in colour differning<br>with dopand concentration | Yes |

Table 1 Technologies Considerations

Table 1 above provides some processing steps that are normally available with silicon technology but are assessed in light of processing SiC. For example common doping techniques in silicon include diffusion, ion implantation and to a limited extent during epitaxial growth. In silicon common n type dopants include Phosphorus, Arsenic and Antimony whereas for p type the most common is Boron.

In 3C SiC the n type dopants include Nitrogen and Phosphorus and p type include Aluminium and Boron. The energy levels within the conduction band sometimes is used for selection, and with Nitrogen being a possible impurity(contaminant) in some processed could be precluded in preference to Phosphorus.

However the introduction of the dopant species while being commonly achieved by ion implantation in silicon is not as attractive for SiC on Si because of the high implant and anneal temperatures, in excess of 1100C and times up to one half an hour each step. Similarly diffusion at reasonable temperatures is almost impossible in SiC. So for doping purposes the most common technique for SiC on Si is through epitaxy which when given the right pressure conditions can be achieved at silicon compatible temperatures.

Oxidation both thermal and chemical vapour is generally compatible with silicon. Oxygen gas additives are also generally similar to silicon and process temperatures of a similar value. Thus for surface oxidation and pre cleaning conventional silicon process equipment will suffice.

Silicon Carbide is well know as a mechanical abrasive, in fact its hardness and inertness make it terribly difficult to work with. When etching for example it is almost chemically inert requiring dry etching technology to remove layers. This then also requires masking materials that will enable fine line etching to occur. Classical masks such as oxides and nitrides must be replaced by other masks such as metal or other hardened films.

Other metals and nitrides can be deposited in a similar way to silicon as is the photolithography requirements.

So equipping of the facility for these technologies will be with 150mm diameter silicon compatible equipment. The main difference being with the doping and deposition technologies and also with the etching technology/ies.

## 4. OPERATING THE FACILITY

Conditions surrounding the SSRFF and the University Building require the QMF to peruse research that is focused and that has potential commercial benefits. It required that funds be sought to further the research and commercialisation of the original stored charge memory patent. The object being to expand the IP portfolio and thus the worth of the QMF.

To achieve this, models of engagement of the QMF for both internal and external projects needed to be developed. This had to be achieved within an internal framework of support for such activities, at Griffith University this involves the interaction of the Office for Research, the Office for Commercialisation as well as of course the Legal Service Unit.

It should also be noted that the QMF is set up as a strategic research centre of the University with a board of management reporting through the Pro Vice Chancellor Science and Technology. The Board has a research sub committee which provides recommendations on research programs as to their relevance and engagement with the QMF. The sub committee apply rigorous selection criteria to projects so that the standards of the QMF are not compromised.

Some examples of possible internal engagement include,
**Join a project team**. From time to time when projects are being scoped there may be a need for certain expertise to be provided as part of the project. Relief from teaching and other duties could be paid to academic staff to enable full time relief to work on the project.
**Propose a project** that could expand the QMF background IP or know how. A project of this type could have funding from ARC discovery grant or equivalent. The QMF would assist researchers identify relevant core areas and assist with the ARC application. From time to time the QMF will circulate these areas and encourage participation through open forum.
**Linkage projects** with industrial participants. Industry participants may from time to time want to leverage research funding for a particular project and use the ARC Linkage program as a means of achieving this. It may also be for the support of a researcher such as an PhD or research fellow, this means will be encouraged by the QMF and assistance again will be provided for this to happen.
**Academics own program**. Academic can suggest their own program that fits the core activities of the QMF. If support cash or in kind can be found the project will be encouraged to be carried out in the QMF.

As far as external projects are concerned the Office of Commercialisation acts as the interface from the University to the outside world We have adopted an engagement model that we refer to internally as the **project model**. The project is commissioned by an external party under the conditions that the project outcomes in terms of IP become the sole property of the University. The contract then outlines the conditions of access to this IP (and background IP). These conditions may be exclusive, first right etc. The contracting partner can engage their own researchers but must do so by enabling them to be University employees so that the IP is exclusively owned. Of course there can be variants to this for example when a contracting body brings along IP, when the University has worked on the project exclusively (eg ARC funded project), when a body has paid for the IP to be generated but has no intention to commercialise the product but will retain some share of the IP etc. In this model RhD students whose project generate IP of value to the project must assign the IP rights to the University in return for some form of return such as a stipend.

These models of engagement require that a project team of skilled and highly trained reserachers can be bought together for the life of the project and often at quite short notice. This often requires short term engagements which is ideal for academics with some form of relief from other duties. However for RhD training purposes it is less than ideal. As a consequence students are generally employed into growing the core IP that will be of benefit to the QMF in the longer term and kept out of commercially sensitive projects. Currently an **Affiliates Program** for RhD support is being put in place to provide support for at least ten RhD students.

Project teams are built with a skill base in mind. Access to the Fabrication area for example is on a qualified user basis as is access to the various testing areas. To this end the actual number of QMF staff is not large, namely project and high level technician support and RhD students. Some academic staff may align themselves permanently with the QMF and thus assume supervision status as well as providing projects to the Facility.

Commercial projects within an academic environment is always a challenging task. However access to the QMF is quite strict and in particular project areas will be highly secure. Of course common use areas such as the fabrication and testing laboratory need special attention and control over possible conflicts.

## 5. THE QMF BUILDING AND EQUIPMENT

Armed with the above information and to fit within a strict budget the following areas have been allocated within the QMF building; 240M2 of fabrication, 80M2 of general laboratory and 640M2 of office and general purpose space. The layout is shown below in figure 4.

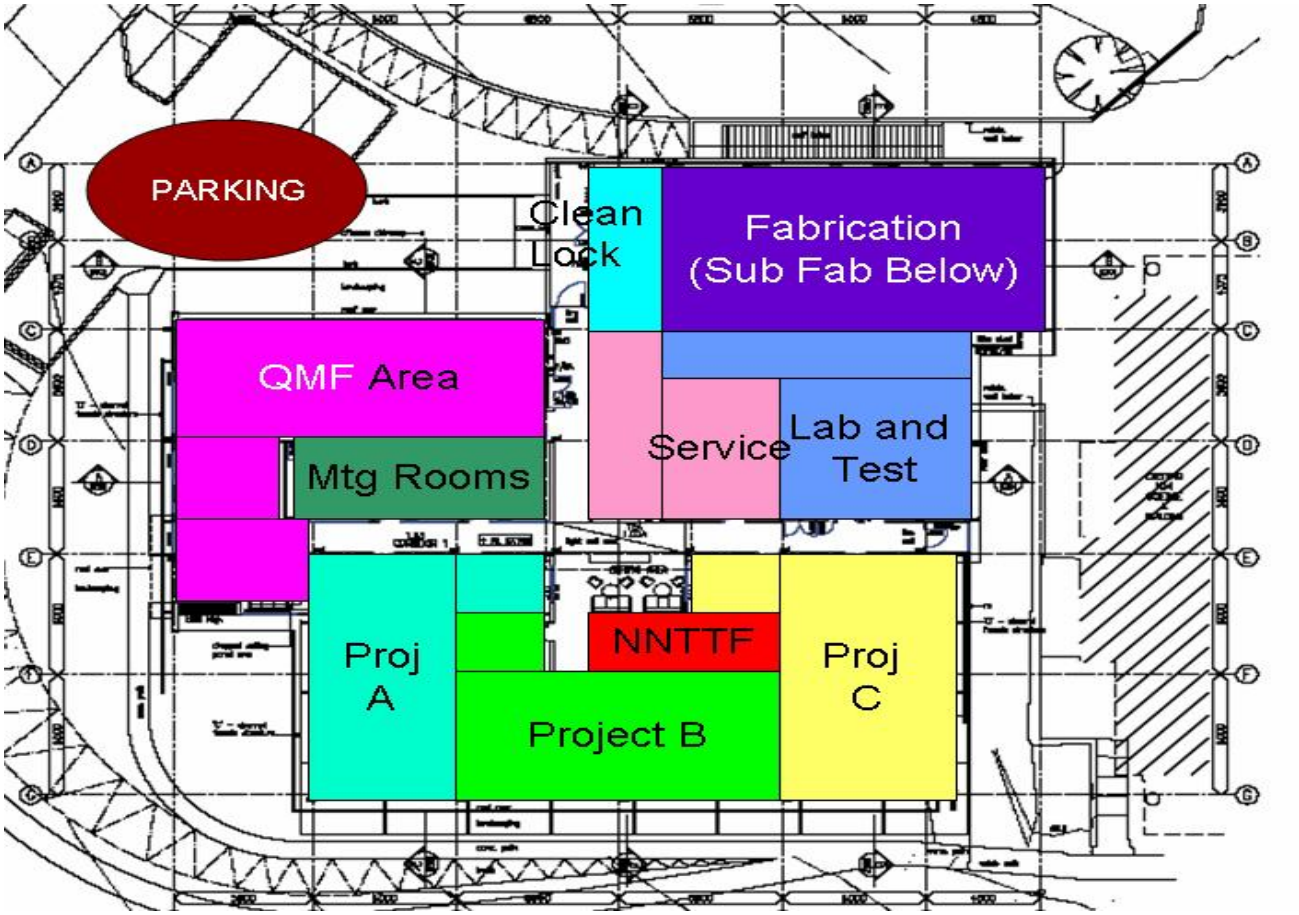


Figure 4 Schematic layout of the ground level of the QMF

The fabrication area is over two levels with the equipment on the top and services on the bottom. In conventional facilities the clean and so called grey areas are on the same level. However due to the natural fall of the land we were able to house the service or grey area under the clean area. The clean area is in a ballroom layout with only the lithographic area being dedicated. The litho area at the eastern end has both temperature and humidity control (for resist purposes). Within the clean area are local class 10 mini environments which service wet and dry processing. All gas handling and distribution and pump services are within the sub fabrication area. A clean shower/gowning area is adjacent to the top clean area.

To complement the fabrication there are two laboratory areas for electrical testing. One is networked to the National Networked Tele Test Facility with the main node at Edith Cowan University in Perth. This is an extensive electrical test facility mainly for systems type testing. This will be used by VLSI post graduate students in the first instance but for extensive system testing of memory circuits when the Facility is more mature. Another electrical testing area is also available closer to the Fabrication laboratory and concentrates more on fundamental testing such as CV, IV and Ct-T, with temperature controlled stages.

Dedicated project areas provide open office and fixed office accommodation for commercial projects and to some extent RhD students. Built along silicon valley office lines these areas are separated form one another and from the QMF offices. Each project can then be self contained, from an office point of view however of course the fabrication and testing areas will be shared.

To complete the facility there are dedicated QMF offices and administration areas as well as meeting rooms that will be of course be shared.

Turning our attention now the equipment requirements for the QMF. We have established that a 150mm diameter wafer facility will suffice. Further with an initial minimum feature size of a little under one micron and with the silicon compatibility established then we have concentrated our attention on acquiring equipment for a full process flow from SiC deposition to final integrated circuit memory cell realisation, as outlined below

EQUIPMENT

Silicon Carbide Specific
Epitaxy and doping furnace/s----Custom built
Etching------Seeking suppliers

General
- <1.0 μm lithography
  - Direct write
  - Mask align (double sided)
- Full process flow – as required for Research and Development
  - Oxide growth , Polysilicon deposition
  - Dielectric and metal deposition
  - Plasma and wet chemical etching etc.

## 6. CONCLUSION

A new and unique semiconductor facility being built at the Nathan Campus of Griffith University has been described. The focus of the facility is toward the development of 3C SiC on Si technology and is being equipped to realise memory device structures in that technology. The new facility to be called the Queensland Microtechnology(QMF) Facility should be operational in the second half of 2006.

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