Assessing the 1/f Noise Contributions of Accidental Defects in Advanced Semiconductor Devices

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ABSTRACT

The effects on the overall device noise of a small number of defects in device sections with a strong transfer impedance coupling to the device terminals is discussed using advanced bulk and silicon-on-insulator n channel MOSFETs and silicon nanowires as examples. From the measured noise and current-voltage data, the precise physical location of the noise centers is determined. Potential noise reduction methods are discussed.

Keywords: Nanowire, silicon-on-insulator CMOS noise, low frequency noise, noise reduction.

1. INTRODUCTION

It is well known that defects and traps distributed in for example the gate oxide of MOS devices or surface passivating layers of other technologies and sufficiently close to the charge transport channels to allow for carrier trapping and detrapping will produce an 1/f low frequency excess noise component that can be understood in terms of the unified carrier number fluctuation model. For a trap distribution homogeneously distributed in space and energy a rather monotonous 1/f like component results with a frequency component close to -1. This ever present noise component negatively affects the signal to noise ratio in the low frequency (LF) base band and in radio frequency (RF) bands via possible up conversion in non-linear circuits. To quantify low frequency noise magnitudes in, for example, the linear regime of device operation, the relative current spectral density, S_i/I^2, may be expressed as $S_i / I^2 = A / f$, where I is the DC current, f is frequency, and A is a constant. If the carriers producing the noise may be considered statistically independent, the constant A may be interpreted as α_H/N where α_H is the Hooge parameter[1] and N is the number of carriers. The Hooge parameter is a convenient noise figure of merit to compare device technologies or devices independent of the 1/f noise producing mechanisms. Clearly with the current aggressive scaling of silicon devices and the introduction of nanodevices such as carbon nanotube FETS and bridging silicon nanowires the value of N becomes smaller resulting in show-stopping levels of 1/f noise for a number of applications. Various studies have successfully addressed lowering the 1/f noise levels via a materials science approach, i.e., reducing the interface defect and trap densities or improving the quality of surface passivation layers by selective annealing.[2,3]

The focus of this paper is on identifying, modeling and discussing a path to reducing the 1/f like noise caused by a small number of accidental defects, generated unintentionally during device fabrication. Our investigations using physics-based numerical device noise simulators have shown that single defects located in bulk and SOI MOS device sections with strong transfer impedance coupling to the device terminal of interest, such as the oxide region close to the source-channel potential minimum, are responsible for generation-recombination noise Lorentzian noise signatures superimposed on a broad 1/f noise background.[4] Clearly defects present in other sections of the oxide and channel do produce microscopic noise via carrier capture and emission, but do not couple effectively out to the drain terminal making their presence less consequential from a noise point of view. A second example is the 1/f noise observed in novel bridging silicon nanowires which can be attributed to the non-idealities of the impinging end of the bridging nanowires.[5] From a materials point of view it may be difficult, impossible or too costly to anneal out a very small number of defects at a very precise location in an advanced device structure. However, a little used electrical method employing pulsed biasing to manipulate trap occupancy and thus noise generation in specific device regions shows promise for noise reduction in as made devices.[6] In the following a detailed description of the reverse engineering process that leads from the measured noise at the device terminals to the physical location of the microscopic noise sources will be presented followed by a discussion of the pulsed bias noise reduction technique.

2. SINGLE DEFECTS IN ADVANCED MOS TRANSISTORS

Earlier noise studies by Hou et al.[7] on nondegenerate bulk nMOSFETs showed that a small number of defects located in the oxide region just above the source channel potential minimum were responsible for distinct Lorentzian generation-

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recombination noise signatures superimposed on a monotonous McWhorter type 1/f noise background. Martin et al.[4] extended this work to include direct tunneling from a degenerate conduction band to traps in the oxide and studied the noise characteristics of nominal 90 nm channel length bulk and SOI nMOSFETs fabricated in the same lot in the same fab process with only the starting material being different. To match the results of the noise measurements the slope of the overall 1/f like noise was matched by adjusting the parameter η of the following trap equation [4]

$$N_{tox}=N_{tox0} * \exp(\eta * \delta x) + N_{disc} \quad (1)$$

where N_{tox0} is the peak volumetric density of traps at the interface, η is the constant of logarithmic proportionality, δx is the trap-interface distance. N_{disc} represents the effective density of discrete traps that were added to match the frequency dependent structures observed in the measured characteristics, with their distance from the interface set to bring about a match of the cutoff frequency of the resulting Lorentzian, and the lateral position to match the drain bias dependence of the observed Lorentzian. The local effective trap density is set to match the low frequency magnitude of these components. Focusing on the bulk devices first, there appear to be traps at three oxide grid locations near the source end of the channel. Finally, by observing the drain dependence of the parts of the noise measurements not dominated by any obvious Lorentzian , the N_{tox0} parameter was adjusted to give a Gaussian distribution in the lateral direction centered toward the drain end. The peak value of N_{tox0} used is $10^{14}cm^{-3}$. This background is interpreted as a few traps in the drain region for which there is not sufficient information in the measured characteristics to discern a finer trap placement. The trap distribution used to fit the measured results is depicted in Fig.1. Trap 1 has a density of $5.10^{18}cm^{-3}$, corresponding to a total number of 4 traps in the 3.2 μm wide device. Traps 2 and 3 are in neighboring nodes and have a density of $2 .10^{17}cm^{-3}$, corresponding to a total number of 0.5 traps. This is interpreted as a single trap, though the spread of the bumps in the measured data is too wide to be considered a single Lorentzian. The spread may be due to the carriers not always tunneling perpendicular to the interface. The distribution of these traps is unique within the framework of the drift-diffusion and process simulation model we used. The factor η needed to match the greater than 1/f dependence in frequency was $4.5.10^{7}cm^{-1}$.

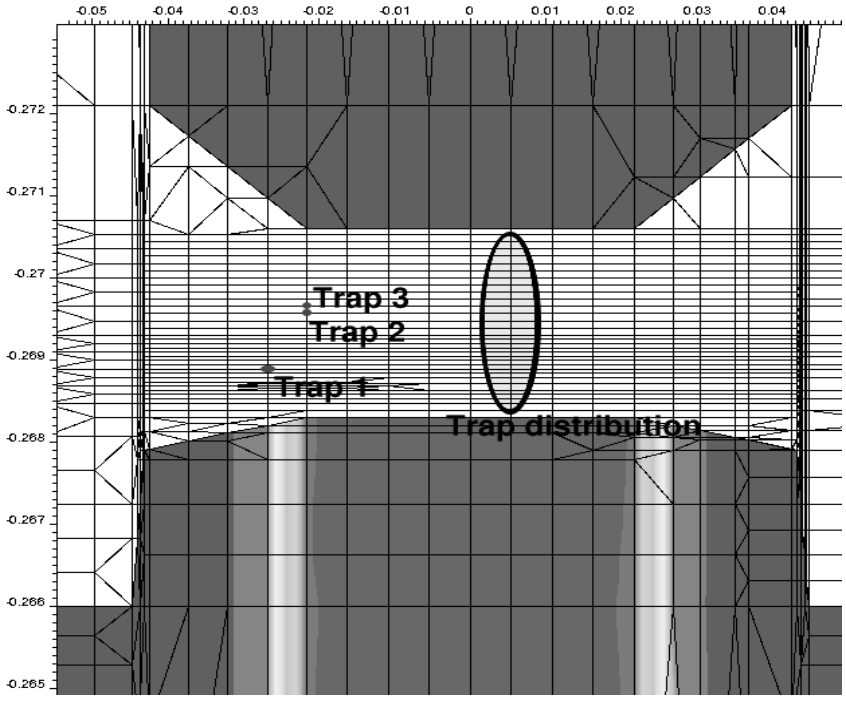

Fig. 1. Graphical depiction of trap locations in the SiO_2 gate oxide. Grey scales indicate net doping densities. The source region is in the bottom left, with the gate above the oxide and the drain region towards the right-hand side of the display. The vertical x-axis and horizontal y-axis are expressed in units of nanometer.

The final fit of the simulated data to the measured data is shown in Fig. 2. No significant diffusion noise was observed in the frequency and bias window chosen for our measurements.

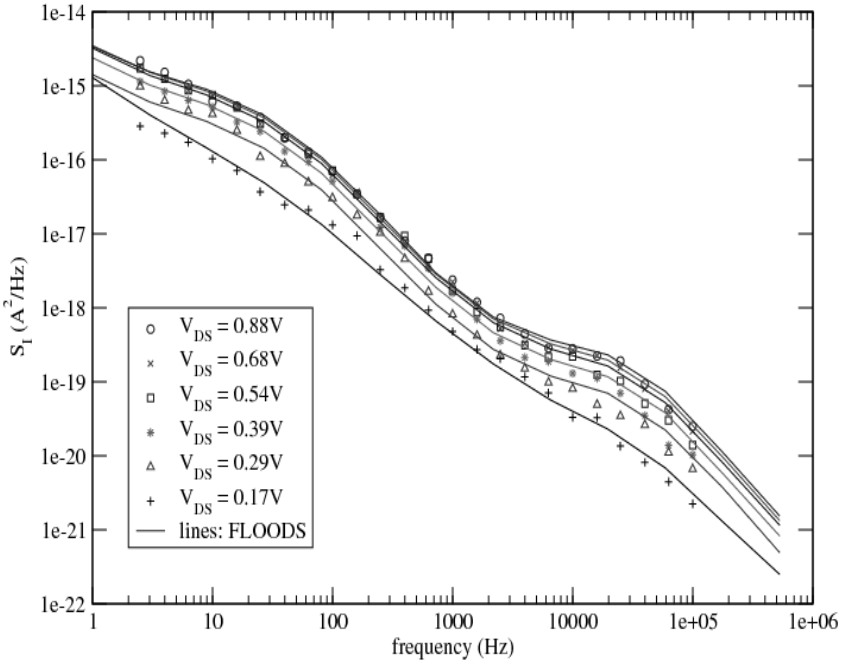

Fig. 2. Measured and simulated current noise spectral density for the 90 nm bulk nMOSFET as a function of drain bias.

Next we turn to the SOI nMOSFET devices. The oxide noise in the measured data is mostly swamped out by the impact ionization initiated diffusion noise charging up the floating body of the FET producing Lorentzian shaped noise components via RC filtering.[8] However some oxide generated noise is apparent, as shown in Fig.3, at high drain bias and low frequency where the impact ionization shifts the excess noise filtered components to low enough zero frequency magnitude so that the oxide noise can exceed it. It is also visible at moderate bias and higher frequencies where the filtered noise rolls off fast as $1/f^2$.

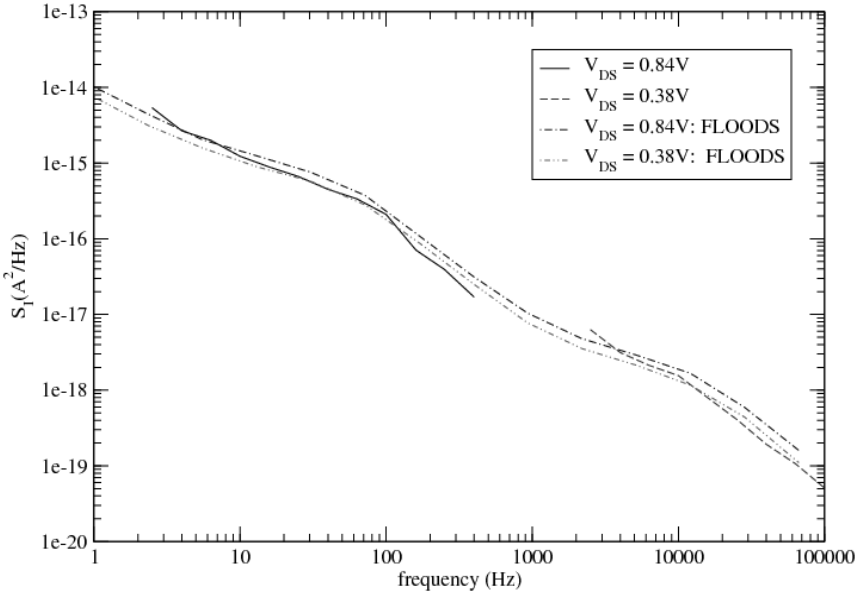

Fig. 3. Simulated and measured oxide noise spectral current density as a function of drain bias for a 90 nm SOI nMOSFET.

The oxide produced noise componets have the same roll off frequencies as the components produced by the traps in the bulk devices so the oxide noise is computed using the trap positions of the bulk devices depicted in Fig.1 and tuning the trap densities and the parameter η to match the increased overall slope of the SOI devices's oxide noise as plotted in Fig. 3. Trap 1 has a density of $5.10^{19}cm^{-3}$, corresponding to a total number of 4 traps in the 4.8μm wide SOI device. Traps 2 and 3 have a density of $1.2.10^{19}cm^{-3}$, corresponding to a total of 1 trap. The peak value of N_{tox0} and η used to match the background noise as in the bulk device were $1.2.10^{15}cm^{-3}$ and $2.6.10^{7}cm^{-1}$, respectively. The similarities between the bulk and SOI device oxide noise are striking, and indicate that the traps near the source/body junction under the gate are most likely a result of the gate oxidation recipe, and/or subsequent processing steps. This analysis does not reveal much about traps present elsewhere in the oxide, however. Additional traps will most likely be present and generate noise at the distributed microscopic level but do not couple out effectively to the contacts in the spectral frequency and bias range used in this study.

3. NOISE IN SILICON NANOWIRES

Silicon nanowire bridges were grown between electrically isolated electrodes formed from the top silicon layer of (110)-oriented silicon-on-insulator (SOI) substrates. Approximately 1 nm Au was deposited on the (111)-oriented sides of the electrodes and annealed in a H_2 ambient at 670 °C to form nanoscale Au-Si alloy catalyst islands. The structure was then exposed to a mixture of 15 sccm SiH_4, 60 sccm HCl, and 30 sccm B_2H_6 (100 ppm in H_2) in a H_2 ambient at 680°C and a total pressure of 1.3 kPa for 30 min to grow nanowires bridging between electrodes with a separation of 10 μm or less. Highlights of the fabrication process for the bridging nanowires are illustrated in Fig. 4.[5] The dimensions of the Si nanowires used in our experiments, were measured using a Scanning Electron Microscope (SEM). Length ranged between $(3\text{-}15)x10^{-4}$cm and radius between $(3.8\text{-}8.3)x10^{-6}$ cm.

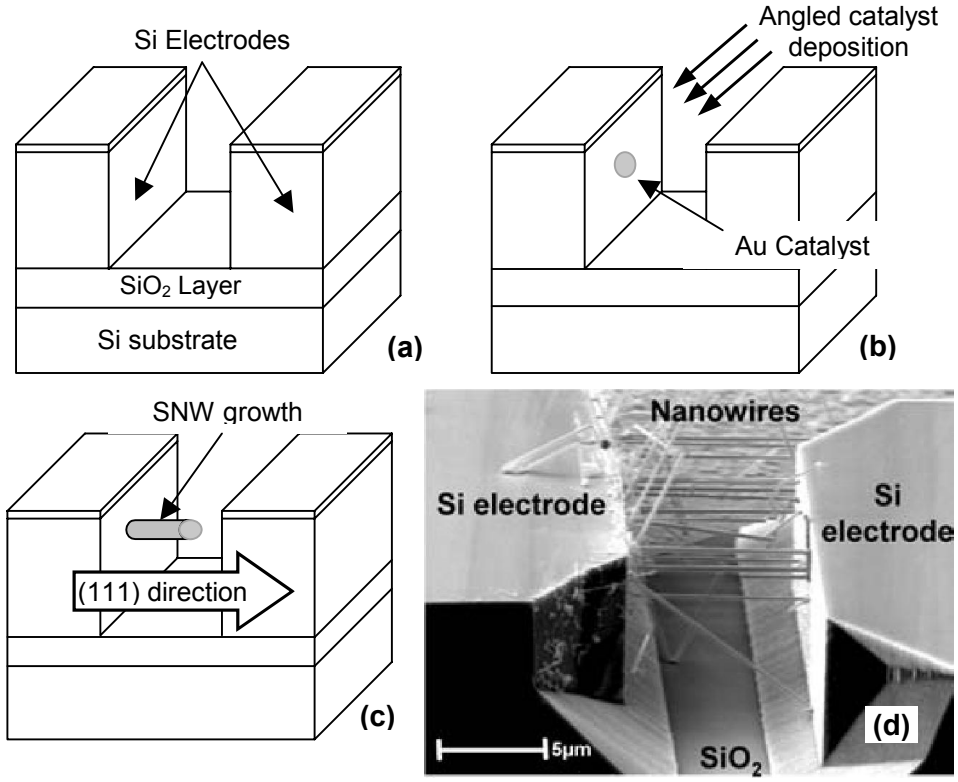

Fig. 4. Illustration of fabrication steps for silicon nanowires; (a) Etching to form electrodes on a SOI substrate (b) Angled deposition of Au catalyst particles and (c) Nanowire growth in (111) direction. SEM image of multiple nanowires bridging across the gap between the Si electrodes shown in (d).[9]

The measured resistivity and the 1/f noise coefficient *A* presented in Fig. 5 show significant variations from device to device. The graph also indicates that the devices from these two wafers studied which have the lowest effective

resistivity also generally show the lowest noise. These devices can be identified as the devices with low contact resistance. The fact that the low-noise devices also have low contact resistance suggests that the source of the noise is the contact. To check this possibility further a lumped noise model will be presented next.

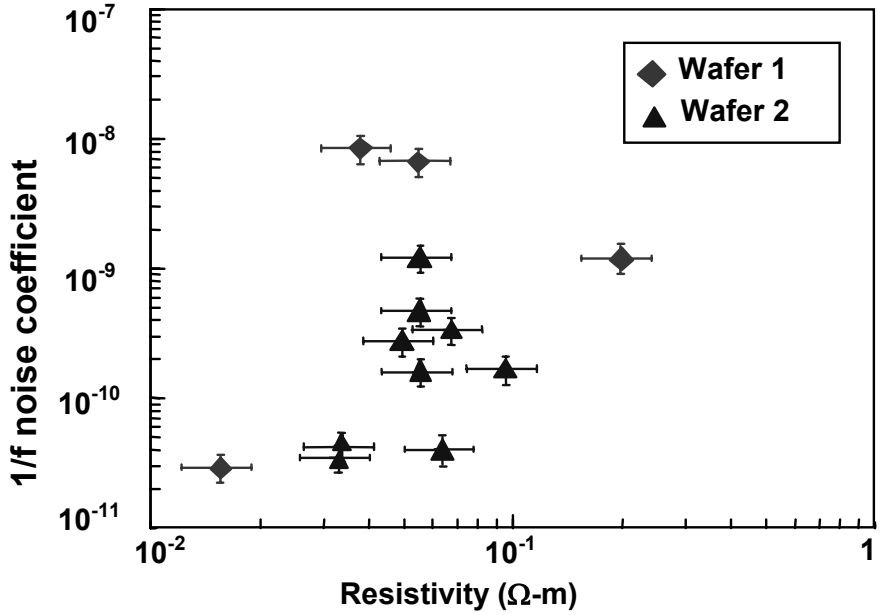

Fig. 5. 1/f noise coefficient A vs. effective resistivity ρ. The uncertainties in A and ρ due to the measurement uncertainties are shown.

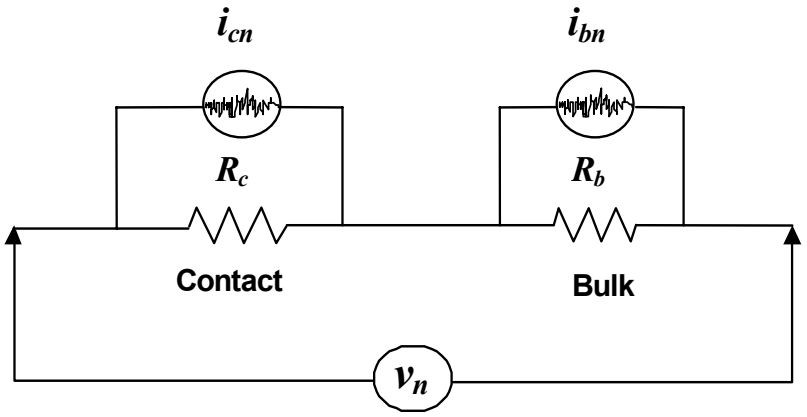

Fig. 6. Circuit representation of the noise model

The proposed noise model includes bulk and contact components just like the bulk and contact components of a resistor. The circuit diagram of the model is shown in Fig. 6. From this circuit, the measured open-circuited noise voltage across the terminals is given by,

$$v_n = i_{bn} \cdot R_b + i_{cn} \cdot R_c \tag{2}$$

where i_{bn} and R_b are the noise current source and the resistance respectively of the bulk region, and $\boldsymbol{i_{cn}}$ and R_c are the noise current source and the resistance respectively of the contact region of a wire.

From Eq. (2) the total 1/f voltage noise spectral density S_v in terms of the individual current noise spectral densities is given by,

$$S_v = S_{ib} \cdot R_b^2 + S_{ic} \cdot R_c^2 \tag{3}$$

where S_{ib} and S_{ic} are the current noise densities of the bulk and contact noise sources, respectively.
From Eq. (3), with the total resistance $R = R_b + R_c$, the total current noise spectral density can be written as,

$$S_i = S_{ib} \cdot \left(\frac{R_b}{R}\right)^2 + S_{ic} \cdot \left(\frac{R_c}{R}\right)^2 \tag{4}$$

Using $S_i / I^2 = A / f$,

$$S_i = \frac{A}{f} \cdot I_{dc}^2 = \frac{A_b}{f} \cdot I_{dc}^2 \cdot \left(\frac{R_b}{R}\right)^2 + \frac{A_c}{f} \cdot I_{dc}^2 \cdot \left(\frac{R_c}{R}\right)^2 \tag{5}$$

where A_b and A_c are the 1/f noise coefficients for the bulk and the contact region, respectively. Eq. (5) can be simplified to

$$A = A_b \cdot \left(\frac{R_b}{R}\right)^2 + A_c \cdot \left(\frac{R_c}{R}\right)^2 \tag{6}$$

Most of the devices studied contained multiple nanowires. For those cases, the total noise of the device is the sum of the noise contribution from all the nanowires in the device. Hence,

$$S_t = \frac{A_t}{f} \cdot I_t^2 = \sum_{i=1}^{N} \frac{A_i}{f} \cdot I_i^2 \tag{7}$$

$$\Rightarrow A_t = \sum_{i=1}^{N} A_i \cdot \frac{I_i^2}{I_t^2} \tag{8}$$

where A_t and I_t are the combined noise coefficient and current for all the nanowires in the device under study and, A_i and I_i are the noise coefficient and current for the *i-th* nanowire. Using Eqs. (6) - (8),

$$A_t = \sum_{i=1}^{N} \left[A_{bi} \cdot \left(\frac{R_{bi}}{R_i}\right)^2 + A_{ci} \cdot \left(\frac{R_{ci}}{R_i}\right)^2 \right] \cdot \left(\frac{I_i}{I_t}\right)^2 \tag{9}$$

From Eq. (9), the bulk and contact noise components can be separated. The bulk noise is given by,

$$A_b = \sum_{i=1}^{N} \left[A_{bi} \cdot \left(\frac{R_{bi}}{R_i}\right)^2 \right] \cdot \left(\frac{I_i}{I_t}\right)^2 \tag{10}$$

and the noise component from the contact is given by,

$$A_c = \sum_{i=1}^{N} \left[A_{ci} \cdot \left(\frac{R_{ci}}{R_i}\right)^2 \right] \cdot \left(\frac{I_i}{I_t}\right)^2 \tag{11}$$

with

$$A_t = A_b + A_c \tag{12}$$

If either A_b or A_c is known, the other one can be calculated from Eq. (12).
The noise component of the bulk can be accurately determined from the devices that have negligible contact resistance. To understand this, consider Eq. (9). For negligible contact resistance, i.e. $R_b >> R_c$, we have $R \approx R_b$ and $R >> R_c$. Then from Eq. (9)

$$A \approx A_b \tag{13}$$

Also, from Eq. (10) with $R_i \approx R_b$,

$$A_b = \sum_{i=1}^{N} \left[A_{bi} \right] \cdot \left(\frac{I_i}{I_t}\right)^2 \tag{14}$$

From the well known Hooge model for bulk 1/f noise,[1]

$$A_{bi} = \frac{\alpha_{Hb}}{p \cdot V_i} \tag{15}$$

where α_{Hb} is the Hooge parameter, p is the density of carriers and V_i is the volume of the i-th wire. Using the Hooge model in Eq. (14),

$$A_b = \alpha_{Hb} \cdot \sum_{i=1}^{N} \frac{1}{p \cdot V_i} \cdot \left(\frac{I_i}{I_t} \right)^2 \tag{16}$$

$$\Rightarrow \alpha_{Hb} = A_b \Big/ \sum_{i=1}^{N} \frac{1}{p \cdot V_i} \cdot \left(\frac{I_i}{I_t} \right)^2 \tag{17}$$

The Hooge parameters were calculated from the devices with the lowest resistivity and noise. As these devices have the lowest contact resistance, the α_{Hb} calculated using Eq. (17) gives the best estimate of the bulk Hooge parameter. The calculated Hooge parameters are 1.1×10^{-5} and 7.5×10^{-6} for wafer 1 and wafer 2, respectively. In general the value of the Hooge parameter is a good indicator of the process quality, and the values obtained for the Si nanowires are comparable to Hooge parameters of modern low noise silicon bulk devices.[10] Using these calculated Hooge parameters the bulk and contact noise A values for the other devices were calculated using Eqs. (10), (11) and (12).

However, unlike bulk noise, there is no known model for contact noise, so the contact noise magnitude per wire (A_{ci}) cannot be calculated directly from Eq. (12). To calculate the contact noise it is necessary to assume a functional dependence between the noise magnitude and some physical parameter such as the radius or length. One can expect the contact noise to be some function of radius but independent of length. Hence, the following model for the contact noise was adopted,

$$A_{ci} \propto r_i^m \tag{18}$$

where r_i is the radius of the nanowire. The exponent m determines how the noise is related to the physical parameter of the corresponding nanowire. For example, for m = 0, 1 and 2, the noise is independent, proportional to the perimeter and proportional to the cross-sectional area respectively. The values for m tested for a fit were –3, -2, -1, 0, 1, 2 and 3. The best fit to the data was obtained for m = -2, in other words the best-fit model suggests the relative noise is inversely proportional to the cross sectional area of the nanowire i.e.,

$$A_{ci} \propto \frac{1}{\pi r_i^2} \tag{19}$$

The proportionality constants for wafers 1 and 2 are 4.7×10^{-18} cm^2 and 4.6×10^{-19} cm^2, respectively. Current-voltage analysis show that the contact resistance is also inversely proportional to the contact area, i.e.,

$$A_{ci} \propto R_{ci} \tag{20}$$

The likely mechanism for contact noise in the case of these nano wires is carrier trapping-detrapping in defects producing the well-known 1/f-like number fluctuation noise spectra. The impinging end of the wire, where contact to the silicon electrode is made through possibly pinholes in the native oxide, is expected to be defect rich and thus the dominant source of contact noise whereas the base end of the nanowire is connected epitaxially to the silicon sidewall creating a defect lean, lower noise contact configuration. Furthermore, because of the higher resistance on the impinging side, any fluctuations in this contact will couple out more to the device contacts.

Because the contact was identified as the dominant source of noise, further noise reduction can be envisioned by optimizing the contact. Reducing the contact resistance can potentially reduce contact noise because they originate from a common mechanism, as indicated by Eq. (20); moreover less contact noise will couple out into the remainder of the circuitry as the contact resistance becomes a smaller fraction of the total resistance.

4. NOISE REDUCTION

To reduce the low frequency excess noise generated by a few traps in very specific device areas two different approaches may be considered. One well established method is to measure the noise and current-voltage characteristics in the bias regime of interest, develop an accurate, physics based LF device noise model using for example numerical simulations based on a Green's function transfer impedance approach as discussed in the nMOSFET example, and subsequently reverse engineer from the measured data the locations where the LF noise is produced. This information

can then be fed back into the device fabrication process so that selective defect reduction techniques such as optimized contact metals, annealing temperatures, and passivation techniques may be applied to both front- and back-end processes as outlined for example in several papers from the IMEC noise group.[2,3] While successes have been achieved, the method may be cumbersome, potentially costly , and may cause conflicts with other fabrication step priorities. A second, less explored, but promising technique is to accept the devices as fabricated and develop a smart, physics-based bias voltage profile to manipulate the charge transfer dynamics of the noise producing defects in such a way that noise reduction results. Bloom and Nemirovsky[11] were the first to report that cycling a MOSFET from strong inversion to accumulation reduced the 1/f noise in some devices more than could be expected based on a reduced duty cycle argument alone. Others confirmed these findings and observed similar results in the behavior of RTS components.[6,12,13] In his dissertation Kolhatkar[6] presents a model relating the observed changes in noise under pulsed bias conditions to the non-stationary values of trap emission τ_e and capture times τ_c under these conditions. In particular the emission time constant is strongly affected by a pulsed gate bias. Typically, the noise magnitude generated by a trap center is a function of emission and capture time constants and reaches a maximum for $\tau_e/\tau_c=1$. Consequently, if pulsed biasing moves the value of this ratio established under dc bias further away from one, a noise reduction results. If however, pulsed biasing effects the emission time in such a way that the τ_e/τ_c ratio moves closer to one, a noise increase will result. Therefore research and a thorough understanding of the noise producing mechanisms is required to design the proper bias signature to achieve a noise reduction and this signal may be different for different technologies. Ideally, this bias signature should be placed in an unused bandwidth portion of the device circuit. The advantages of this method are that it can be applied at little expense to devices after fabrication and addresses an electrical problem with electrical means whereas materials science techniques may affect more than just the electrical performance of a device.

REFERENCES

1. F. N. Hooge, "1/f noise is no surface effect," Phys. Letters, 29A, 139-140 (1969).
2. C. Claeys and E. Simoen, "Impact of advanced processing modules on the low-frequency noise performance of deep-submicron CMOS technologies," Microelectronics. Reliability 40, 1815-1821 (2000).
3. C. Claeys, A. Mercha and E. Simoen , Low frequency noise assessment for deep submicrometer CMOS technology nodes," J. Electrochemical Society, 151 (5) G307-G318 (2004).
4. D. O. Martin, "Simulation of noise mechanisms in scaled bulk and partially depleted silicon-on-insulator field effect transistors," Ph. D. Dissertation, University of Florida, USA, 2007.
5. S. Reza, "Excess noise in one dimensional quantum nanowires," Ph. D. Dissertation, University of Florida, USA, 2006.
6. J. S. Kolhatkar, Steady-state and Cyclo-stationary RTS Noise in MOSFETS, Ph. D. Dissertation, University Twente, The Netherlands, 2005.
7. F.-C. Hou, "Low-Frequency Bulk and Surface Generation-Recombination Noise Simulations of Semiconductor Devices," Ph. D. Dissertation, University of Florida, USA, 2002.
8. G. O. Workman, "Physical modeling and analyses of deep-submicron silicon-on-insulator CMOS devices and circuits," Ph. D. Dissertation, University of Florida, USA, 1999.
9. M. S. Islam, S. Sharma, T. I. Kamins and R. Stanley, "A novel interconnection technique for manufacturing nanowire devices," Appl. Phys. A, 80, 1133-1140 (2005).
10. Noise and Fluctuations, Proceedings of ICNF 2005. Editors: T. Gonzalez, J. Mateos, and D. Pardo. AIP Conference proceedings 780, New York (2005).
11. I. Bloom and Y. Nemirovsky, 1/f noise reduction of metal oxide semiconductor transistors by cycling from inversion to accumulation," Applied Physics Letters, 58(15), 1664-1666 (1991).
12. B. Dierickx and E. Simoen, "The decrease of random telegraph signal noise in metal-oxide-semiconductor field-effect transistors when cycled from inversion to accumulation," Journal of Applied Physics, 71(4), 2028-2029 (1992).
13. A. P. van der Wel, E. A. M. Klumperdink, S. L. J. Gierkink, and H. Wallinga, "MOSFET 1/f noise measurements under switched bias conditions," IEEE Electron Device Letters, 21(1), 43-46 (2001).