

Evolution in the concentration of activities in lithography

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ABSTRACT

From a perusal of the proceedings of the SPIE Advanced Lithography Symposium, the progression of new concepts in lithographic technology can be seen. A new idea first appears in a few papers, and over time, there is an increase in the number of papers on the same topic. Eventually the method becomes commonplace, and the number of papers on the topic declines, as the idea becomes part of our industry's working knowledge. For example, one or two papers on resolution enhancement techniques (RETs) appeared in the proceedings of the Optical Microlithography Conference in 1989 and 1990. By 1994, the total number of papers had increased to 35. Early lithographers focused on practical issues, such as adhesion promotion and resist edge bead. The introduction of simulation software brought on the next era of lithography. This was followed by a period of time in which RETs were developed and brought to maturity. The introduction of optical proximity corrections (OPC) initiated the next major era of lithography. The traditional path for scaling by using shorter wavelengths, decreasing k_1 and increasing numerical aperture has given way to the current era of optical multiple patterning and lithography-design co-optimization. There has been sufficient activity in EUV lithography R&D to justify a separate EUV Lithography Conference as part of the annual Advanced Lithography Symposium. Each era builds on the cumulative knowledge gained previously. Over time, there have been parallel developments in optics, exposure tools, resist, metrology and mask technology, many of which were associated with changes in the wavelength of light used for leading-edge lithography.

Keywords: Lithography, OPC, RET, EUV

1. INTRODUCTION

Over time, there has been an evolution in the types of problems that have been the focus of lithography R&D. (Fig. 1) An example of the rise of activity on a specific topic in lithography R&D over a period of time is illustrated in Fig. 2. A few papers on resolution enhancement techniques (RETs) were presented at the SPIE Advanced Lithography Symposium in 1989 and 1990, and this was followed by several years of a much higher level of activity. Early lithographers worked on solutions for practical problems. Theoretical modeling was introduced and developed over time to greater levels of sophistication, eventually resulting in the resolution enhancement techniques (RETs) and optical proximity corrections (OPC) that are in common use today. During the time periods in which these methods were being developed, numerous research and development engineers at multiple companies worked on them. In this paper, the evolution of activity in lithography R&D will be described.

2. PRIOR ERAS OF LITHOGRAPHY R&D

2.1 The practical era

Successful application of lithography to semiconductor processing required that a number of practical problems first be solved. This will be illustrated by two examples. The first example involves a well-known phenomenon that is addressed in the processing of photoresist, that of edge-bead, where a thick ring of resist is created at the edges of wafers when resist is spin-coated. This edge-bead can be problematic, leading to defects and focus issues if not removed. Consequently, special techniques have been developed for removing the edge-bead.¹ In the early days of semiconductor lithography, the edge-bead was large. During investigations into the impact of the shape of the wafer edge on edge-bead it was found that beveled wafer edges resulted in smaller edge-bead.² Moreover, it was also found with beveling that the elimination of the sharp corner at the wafer edge resulted in significantly reduced wafer breakage, providing additional motivation for beveling wafers at the edge.

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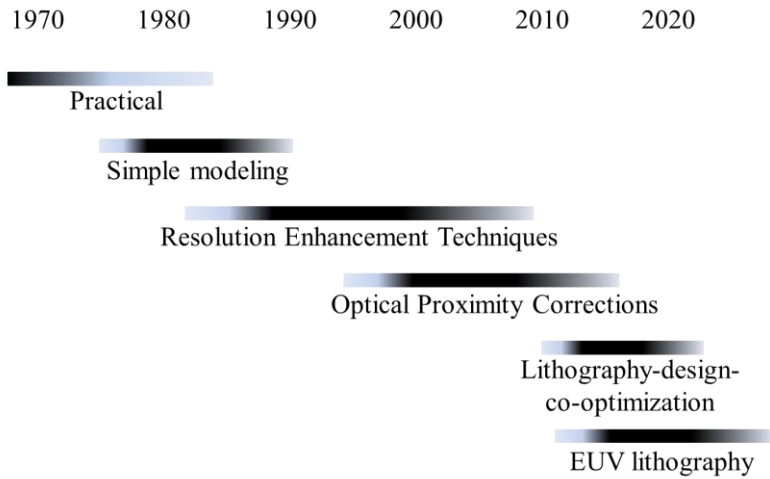


Figure 1. Periods of intense activity of lithography R&D.

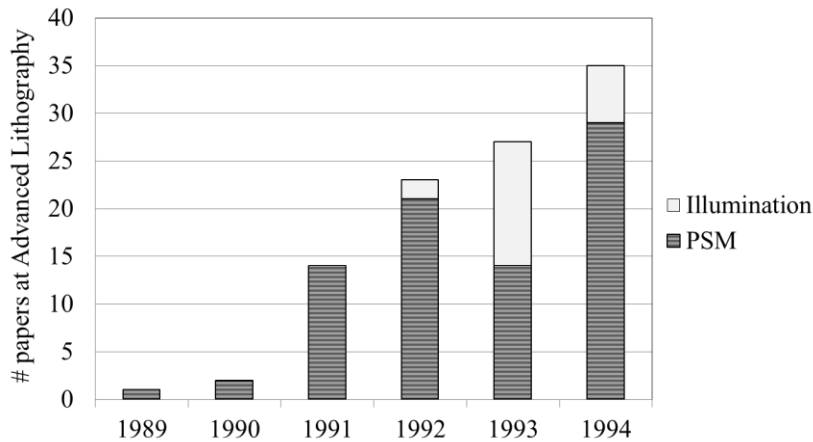


Figure 2. The number of papers presented at the SPIE Advanced Lithography Symposium on the topic of resolution enhancement techniques.

Another practical problem addressed several decades ago was related to adhesion promotion. Hexamethyldisilazane (HMDS) had long been used to promote the adhesion of photoresist. Initially, HMDS was applied in liquid form to wafers immediately prior to resist coating. The HMDS was somewhat effective at displacing the water physisorbed on the wafer surface, but only partially so. An improved adhesion promotion process, needed for ensuring adhesion of the smaller features that were being patterned as a result of scaling, consisted of first heating the wafers in a vacuum to drive off the water, and then introducing the HMDS in vapor form. Initially, vapor priming was a batch process, with cassettes of wafers placed into ovens. (Fig. 3.) Later this technique was adapted for integration into wafer track processing tools. The vapor prime process had several advantages over the prior application of HMDS in liquid form. First, the increased degree of water displacement improved the efficacy of adhesion promotion, which became necessary as feature sizes became smaller. The application of HMDS in vapor rather than liquid form resulted in fewer defects, and it reduced chemical consumption.



Figure 3. A vapor prime oven from Yield Engineering Systems.³

2.2 Early modeling and simulation

A significant advance in lithographic technology occurred when theoretical simulations were introduced, starting with a model created for characterizing positive resist photochemistry by Dill and co-workers.⁴ This was followed by the creation of SAMPLE, which was an early computer program for simulating projection lithography.⁵ SAMPLE was accessible by many lithographers, enabling the widespread use of simulation for understanding problems in lithography. The power of simulation was manifested early. For example, there had long been speculation that optical lithography would be limited by depth-of-focus and would need replacement by other lithographic technologies, such as x-ray or e-beam lithography. Early simulations showed that optical lithography was quite extensible by use of shorter optical wavelengths and practical increases in numerical aperture.⁶ Early exposures using shorter wavelengths did not provide as much improvement in resolution as expected from consideration of optical images, but application of the Dill model revealed the need to optimize resist optical parameters.⁷ Building on the foundation established with SAMPLE, additional simulation programs became available, increasing further the application of modeling and simulation for understanding and solving problems in lithography.⁸

Thin film interference effects and high reflection from substrates coated with aluminum films were problems for early stepper lithography. (Fig. 4) SAMPLE and other early simulation software could be used to predict standing waves and other manifestations of substrate reflections, but often merely the application of simple equations enabled the identification of solutions to problems resulting from reflections from the substrate.⁹ As simple as this modeling was, it differed from the earlier era of lithography, in which few equations would appear in papers on lithography.

In keeping with the increased focus on numerical calculations, process monitoring also became more quantitative. Early process control monitors were often of a pass/fail nature, and sometimes involved only visual inspection of monitor structures, rather than parametric measurement. This situation changed rapidly, and there was sufficient interest in measurements that a stand-alone metrology conference was added to the SPIE Advanced Lithography Symposium in 1987. Quantitative measurements were critical for improvements in process control, starting with the application of basic statistical process control and leading eventually to automatic process control.¹⁰

2.3 Resolution enhancement techniques

Investigations into imaging led to the discovery by lithographers of earlier work by microscopists on the use of off-axis illumination for enhancing resolution.^{11, 12, 13} Nearly concurrent with interest in off-axis illumination was heightened interest in phase-shifting, a technique that had been introduced earlier.¹⁴ The increase in the amount of activity in resolution enhancement R&D is illustrated in Fig. 2. Only one or two papers on RETs appeared at the SPIE Advanced Lithography Symposium in 1989 and 1990, but this number quickly increased to over 20 papers by 1992. The graph in Fig. 2 exemplifies how a good idea becomes recognized and leads to widespread activity on the method. Investigations

into RETs relied heavily on simulation, illustrating how one set of improvements in lithography was based on earlier advances.

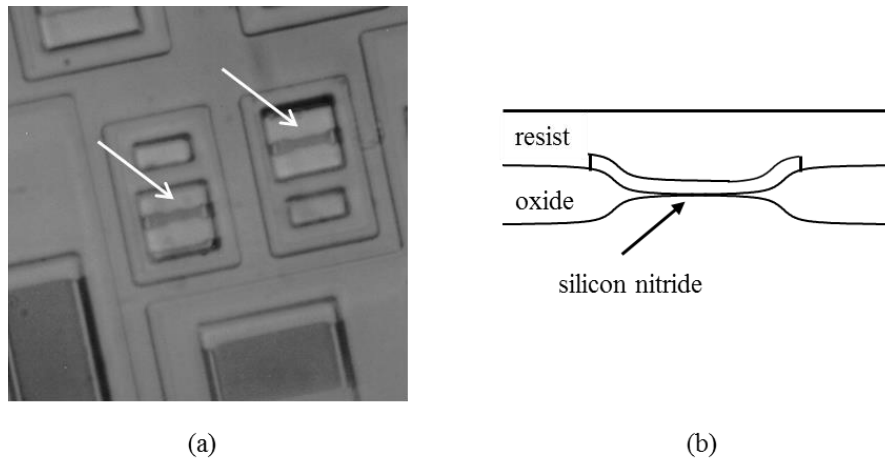


Figure 4. (a) Micrograph of a pattern after etch. The feature was patterned using an 0.3 NA g-line stepper. The arrows show a region where the linewidth varies considerably across the length of the feature, a consequence of thin film optical effects. (b) Schematic cross section of the region indicated by arrows in (a). Because of the variations in thin film thicknesses, the reflections from the substrate varied considerably, leading to the poor patterning indicated in (a).

There were additional consequences to theoretical explorations of RETs. The simulations showed what types of exposure conditions were required for good resolution and depth-of-focus, and these provided guidance to the makers of exposure tools on what hardware enhancements were needed. For example, earlier models of wafer steppers had fixed numerical aperture and conventional illumination with fixed partial coherence. This gave way to wafer steppers that had variable numerical apertures and variable partial coherence. Later, exposure tools with annular and other forms of off-axis illumination became available.¹⁵

2.4 Optical proximity corrections

As capabilities improved for resolving small features, a new set of phenomena started to be observed. For example, when printing lines with identical mask dimensions, the resulting linewidths were dependent upon whether the line was isolated from other patterns or part of a dense pattern. It was possible to compensate for this effect by adjusting the dimension of the features on the mask, depending upon their proximity to other features. This compensation came to be known as optical proximity¹⁶ corrections, or OPC.

There were other types of patterns, besides long lines, in which it was found efficacious to modify the pattern on the mask in order to print something on the wafer that more closely approximated the designer's intent. For example, it was long noted that square patterns on masks printed as circles on wafers, with the high spatial-frequency corners being optically filtered.¹⁷ Others noted that when trying to print rectangles, if the narrow dimension was printed on target, the longer axis would print too short.¹⁸ A way to fix this problem was to lengthen the rectangles on the mask so a pattern with the desired dimensions would be printed on the wafer. Similarly, adding serifs to the corners of squares on the mask would allow for printing less round patterns on the wafer. Although these issues with shortening and corners were not a consequence of proximity of one pattern shape to another, the modifications to the mask to achieve a desired shape on the wafer have still come to be referred to as optical proximity corrections, or OPC. The number of papers on OPC presented at the SPIE Advanced Lithography Symposium is shown in Fig. 5. There was a significant jump in the number of papers between 1993 and 1994, with some fall-off after 1995. With continuing advances, OPC remains a topic of papers presented at the SPIE Advanced Lithography Symposium.

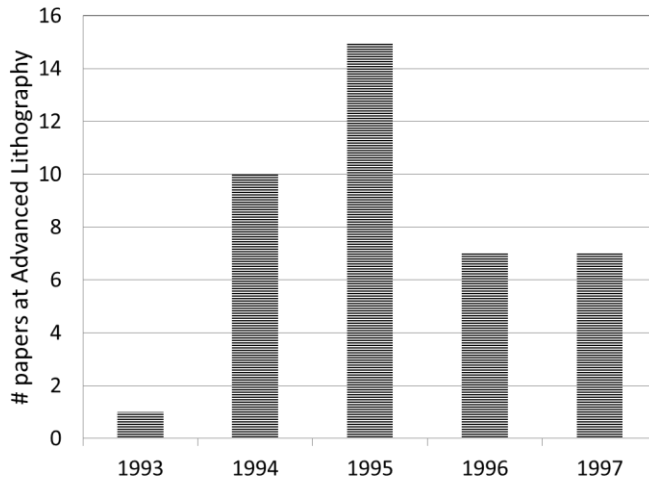


Figure 5. Number of papers on OPC in the proceedings of the SPIE Advanced Lithography Symposium.

2.5 Lithography-design co-optimization

During the transition between 45-nm and 32-nm logic nodes there was not a concurrent significant increase in the resolution of optical exposure tools. As a consequence, to achieve the desired pitches, patterning was required at values of $k_1 = 0.35$ and lower. Even with well-stocked RET and OPC toolboxes, at such values for k_1 it became impossible to pattern logic layouts that were direct shrinks of prior designs or ones with only minor modification. This necessitated substantial changes in design styles, and close interactions and cooperation became required between lithographers and designers. For example, unidirectional lines and spaces are more easily patterned at low values of k_1 than complex 2-dimensional shapes. However, significant layout effort was required to avoid enlarged logic cells with this new design style.¹⁹ Sometimes it was necessary to add levels to the process in order to achieve desired cell sizes, but this would add to overall wafer costs.

The need for greater collaboration between lithographers and designers took another quantum leap with the introduction of multiple patterning.²⁰ In addition to the usual design-rule restrictions based on feature size and shape, specific layouts that could not be composed into two patterning steps became prohibited. Electronic design automation (EDA) tools that traditionally had been solely the province of designers needed inputs from lithographers for applications involving interconnects made with multiple patterning.

Defining new technology nodes has become increasingly complicated. Because of design restrictions, shrinks are no longer proportional to changes in pitches. Rather, the size of actual logic and memory cells needs to be determined, after which routing efficiency needs to be calculated. In combination with estimations of wafer costs, the value proposition of a new technology node, in terms of cost per transistor, can be determined. (Fig. 6)

3. EUV LITHOGRAPHY

An additional set of lithography R&D activities has focused on changes in the wavelength used for leading-edge lithography, and there have been several such transitions since the first use of wafer steppers as exposure tools. With each transition associated with a new exposure wavelength, new capabilities are required in resists, masks, exposure tools, metrology and process control, so each transition is accompanied by a significant amount of research and development in lithography at the new wavelength. Shown in Fig. 7 is the trend in the number of papers on DUV lithography in the SPIE Advanced Lithography Symposium proceedings. For DUV lithography, the increase in the number of papers was more gradual than for RETs, shown in Fig. 2. This was a consequence of a significant number of issues encountered in the early days of DUV lithography, such as poor laser reliability and resist t-topping. It should be noted that the number of papers involving deep-UV lithography eventually grew very large, but often the wavelength

aspect of the papers was not referenced, since deep-UV wavelengths became standard for leading-edge lithography for a period of several years, and the actual focus of those papers was often some other aspect of lithography, such as overlay or design-for-manufacturability.

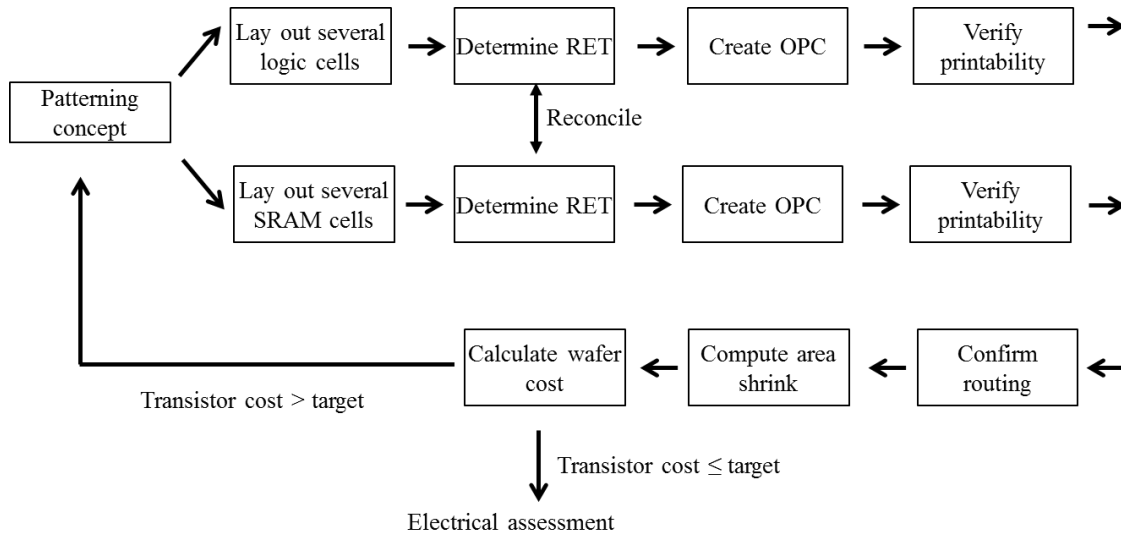


Figure 6. Work process flow for deciding on new patterning concepts. The RET used for logic and SRAM cells needs to be the same, so teams working on the two types of cells need to converge to a single RET.

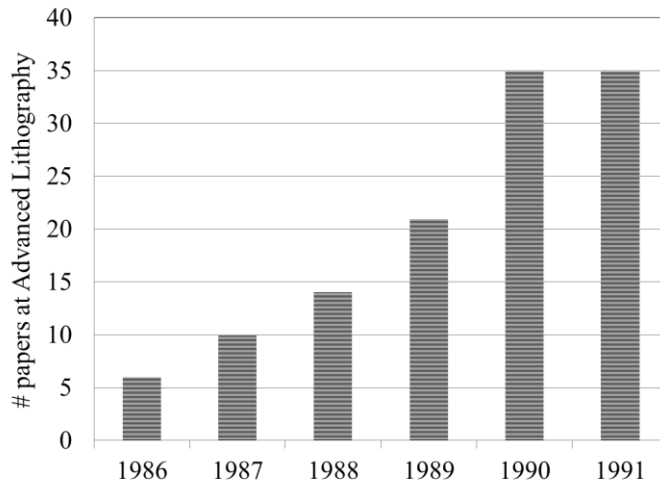


Figure 7. Number of papers on DUV lithography in the SPIE Advanced Lithography Symposium proceedings.

The transition from immersion ArF lithography to EUV lithography is the most recent change of wavelength under consideration. EUV lithography has been the subject of increasing levels research and development, and by 2010 there were sufficient submissions to the SPIE Advanced Lithography Symposium that a separate EUV Lithography Conference was warranted. Additionally, in the 2016 Symposium, on the topic of EUV resist materials, there are multiple joint sessions between the EUV Lithography and Advances in Patterning Materials and Processes Conferences. Similar to the situation encountered previously with DUV lithography, the magnitude of the challenges associated with

EUV lithography has resulted in a state where the number of papers on EUV lithography has remained high and is not expected to taper rapidly, as was the case for several of the other topics that were the focus of R&D interest over short periods of time but then became part of background knowledge.

4. WHAT IS NEXT

With the resolution provided by the short EUV wavelength, aerial images of very small features by projection lithography are made possible. For example, 20 nm pitches can be resolved with a k_1 of 0.35 and a numerical aperture of 0.5. However, full “entitlement” of EUV’s optical resolution has not been yet achieved with current 0.33 NA tools. With a k_1 of 0.35 and a numerical aperture of 0.33, 28 nm pitch resolution should be achieved, but pitches >30 nm are typically achieved, at least with good pattern fidelity. One factor limiting usable resolution is line-edge roughness (LER). It has become appreciated that LER results in large measures from quantum effects, such as photon shot noise and molecular inhomogeneity. As dimensions shrink, such effects can only increase in significance.

For example, it is worth considering length scales. An adamantane molecule, a common constituent of photoresists, is shown in Fig. 8. Such a molecule is 0.5-0.6 nm long. With nominal features that are 10 nm wide, a single molecule represents 5-6% of the linewidth. Achieving low levels of LER will clearly require considerations at the meso-molecular, if not molecular scale. Further scaling will require that molecular-level effects and their manifestations on process control be addressed.

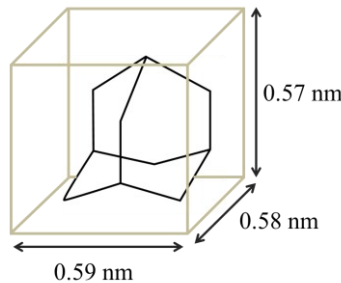


Figure 8. Adamantane molecule, a molecule often found in 193-nm and EUV resists.

5. SUMMARY

At different points in time lithographers have focused on a variety of technical problems, appropriate and pertinent for those times. The solutions that were generated were not just applied and then left behind, but instead they have been added to the base of knowledge for lithographers to make further advances. Today’s focus is on EUV lithography, but requires solutions of practical issues and will require the application of advanced resolution enhancement techniques, OPC and lithography-design co-optimization. The manifestations of molecular-level effects have also become evident when trying to take full advantage of the optical resolution potential of EUV lithography.

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