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HIGH SPEED, HIGH FREQUENCY ELECTRO-PHOTONIC ADC FOR SPACE ENABLED ROUTERS AND FLEXIBLE ANTENNAS

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I. INTRODUCTION

The trend in future telecom satellites is to employ increasingly powerful digital payloads for antenna beam forming and switching. One of the consequences of this trend is that there is a push in satellite communication payload and antennas design towards digital signal processing at higher frequencies. This has a direct impact on the ADC design as conversion bandwidth is limited and has to be traded off with resolution. Within the FP7 project PHASER a space-grade, high speed digitizer capable of direct RF-sampling up to Ka band signals, exhibiting an improvement of more than two order of magnitude in the digitizer frequency response respect to the SoA is being developed, which enables a dramatic hardware complexity reduction for the next generation satellite payloads. The direct RF-sampling is carried out by electro-optically mixing the RF signal with a train of very short optical pulses with pulsed duration and jitter in the range of femtoseconds. The amplitude of the RF signal is translated to the optical pulses (sampling process) and this amplitude information is read in an ADC circuitry. The optical sampler act as a sample-and-hold photonic circuit that is the front-end of the ADC that interfaces directly with the antenna signal. The optical pulses come from an optical clock based on a mode-locked laser. This optical clock is distributed in an optical fibre network to all the optical samplers and ADCs in a synchronized architecture. Preliminary tests on the PHASER demonstrator have demonstrated the capability of digitalization of RF signals from L to Ka band at 2.6 Gsps. This sampling rate enables to digitize the complete Ka-band (1GHz) without frequency conversions. The digitalized signal can be filtered, channelized, frequency converted or processed in general digitally. This technology enables the use of the sub-sampling technique up to millimetre-wave frequencies without adding distortion, resulting in a generic solution for any space application requiring the RF signal digitalization, with a huge reduction in the hardware complexity comparing the traditional implementations.

II. TRADITIONAL ELECTRONIC ANALOG-TO-DIGITAL CONVERSION

Subsampling RF/microwave signals by using electronic ADCs without down-converter stages is the straightforward method for the signal digitalization in a cost effective way. However, a major difficulty encountered is the maximum input frequency that ADCs are capable to sample with enough vertical resolution (number of effective bits). Electronic Track-and-Holds were born to overcome this limitation, unfortunately bringing up further problems. An overview of each technology's limitations is presented below.

A. ADC intrinsic limitations

Typically, the electronic ADCs have a limited input bandwidth and only some models have capabilities of sub-sampling over the second Nyquist band, which corresponds to frequencies above twice the sampling rate.

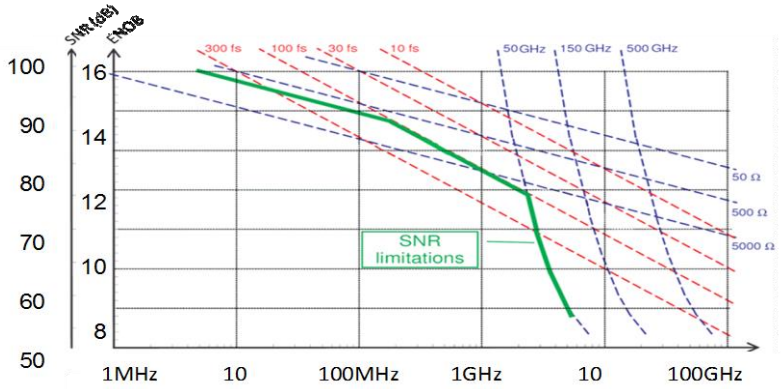

Fig. 1 SNR limitation as a function of the frequency sampling

The main limits imposed to ADC electronics are the following:

1) Noise contributions (thermal, shot, flicker, …) mostly affecting ADC resolution at lower frequencies.
2) Jitter. The uncertainty due to the clock phase noise limits the accuracy when sampling the input signal, which directly affects the maximum input frequency in the ADC.
3) Ambiguity. Circuits in charge of comparisons between the input signal and certain references need some time to generate the digital signal and recover from the comparison. Ambiguity is the main limitation at high frequencies.

Fig. 1 shows the effect of these three limits on the performance for a first order Nyquist band ADC. Few ADCs are capable of reaching more than 10 GHz of maximum input frequency. Specifically, the highlighted line shows the SNR/ENOB limits for an ADC with 1 kΩ input thermal resistor, jitter of 100 fs and 50 GHz of transition frequency.

To overcome the limitations of a single ADC, usually more complex architectures are used. These include enhanced sub-sampling ADCs and multichannel architectures [1]. The first group combines the sub-sampling technique with additional processing techniques to reduce quantization noise. In this way, resolution improves with regard to Nyquist frequency ADCs, although at the expense of bandwidth. Multichannel architectures use N parallel ADCs instead of one ADC. These architectures are used for extending the ADCs performance to higher sampling frequency applications. Nevertheless, multichannel architectures involve bigger physical structures, and misalignments between channels degrade resolution as well.

B. Electronic Track-and-Holds

The traditional solution to increase the maximum frequency that can be digitalized by ADCs is basically implemented employing electronic Track-and-holds, which enable the fast sampling of the RF signals and are placed as an analog front-end of the ADC. These components are optimized to achieve good behaviour at high frequencies allowing the direct digitalization at frequencies of dozens of GHz. Nevertheless, the electronic T&H presents the characteristics of having a limited dynamic range at high frequencies. This limited performance is due to intrinsic limitations of the sampling electronics. Although the evolution of electronics is addressing these limitations as can be seen in Fig.2, in which the spurious free dynamic range (SFDR) of a state-of-the-art T&H from Teledyne [2] is shown, exhibiting a dynamic range dependent from the frequency from 55 to 35 dB for large signal amplitude, the broadband operation at large dynamic ranges is limited.

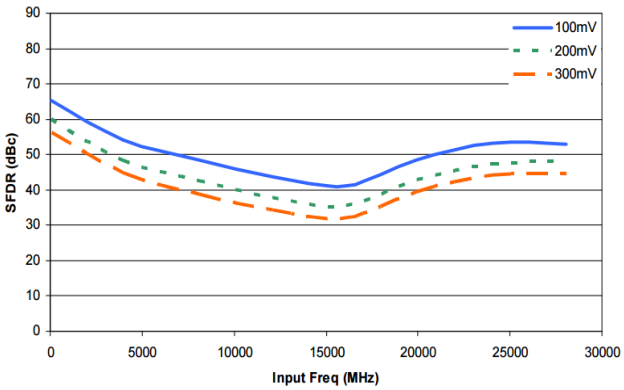

Fig. 2. SFDR vs Input Frequency of the T&H RTH090 from Teledine.

III. OVERVIEW OF PHOTONIC-ADC ARCHITECTURES

In order to overcome the limitations of the electronics ADCs and the T&H, different photonic structures have been analyzed [3-5]. These are briefly presented here.

A. Photonic Assisted ADCs

The first method within Photonic Assisted ADCs basically improves the effective frequency by reducing the bandwidth of the input RF signal and using a slower electronic ADC afterwards. With a stretching factor of M, induced by fiber dispersion effect [9], the effective sampling frequency of the electronic digitizer (fs) is increased up to M•fs. The effective input bandwidth is also increased (M times) and the jitter error from the sampling clock is therefore reduced. Nevertheless, the extremely high optical power needed to reach the necessary average power in the fibre causes large power consumption and non-linearity problems.

The second method of Photonic Assisted ADCs, the optically aided sampling circuit, uses an optical clock generation in order to reduce the sampling jitter, but utilizes the same electronic circuitry, performing both sampling and quantization in electronic domain. In consequence, the only improvement in comparison to the

whole electronic digitizer is of jitter, but not the distortion caused by the electronics with faster signals. This reduces the effective number of bits at signal frequencies above 10 GHz and it worsens at higher frequencies.

B. Photonic Sampling ADCs

The typical approach to implement a photonic sampling ADC architecture is based on a mode-locked laser, a LiNbO Mach-Zehnder modulator and a photodetector. These architectures benefit from the advantages offered by these optical components, which makes the photonic sampling ADCs being the most studied and implemented architectures.

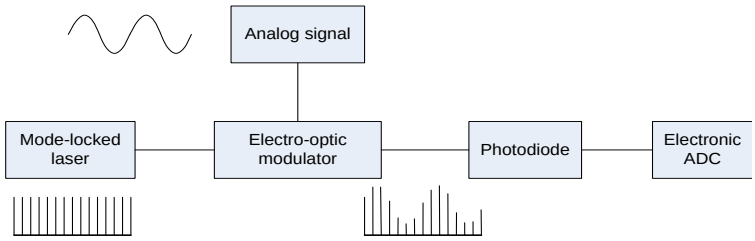

Fig. 3. General architecture of a photonic sampling ADC

The use of mode-locked lasers to perform the optical sampling benefits from the low jitter and narrow pulse width characteristic in these devices, which alleviates the SNR limitations at high frequencies, mainly imposed by timing jitter and distortion of electronic devices. This improvement together with the linear response of high performance photodiodes and the high bandwidth of Mach-Zehnder modulators, makes possible to raise the dynamic range up with regard to other architectures, extending the maximum analog input frequency up to ~100 GHz (limit imposed by the modulator technology, which provides off-the-shelf 100 GHz devices).

The pulse demultiplexing variant is a derived sampling architecture based in several branches, which is used to help the ADC when the sampling rate must be higher, because its sampling frequency shall be equal to the laser frequency. The issue is that lasers can increase it easily, but the ADC not; therefore several time-interleaved ADCs would be needed in this case.

C. Photonic Sampling and Quantization ADCs

In this type of ADCs there are mainly three architectures: Intensity modulation, Sigma-Delta modulators and Optical beam steering.

With regard to intensity modulation it is worth pointing out that it is the first approach in photonic sampling and quantization, being the Taylor's scheme the most well-known approach. This structure brought very interesting results but it had a very limited resolution (4 bits) [7].

The complexity of this system to achieve more than 4 bits makes it not suitable for space and defence applications.

As for Sigma-Delta modulators [1], they are a completely different approach. They are comprised mainly by an integrator, a quantizer, an adder and a 1-bit DAC. The resolution restriction in this architecture is not as limiting as in intensity modulators, but the increase in effective bits is made at the expense of ADC bandwidth. The complexity of performing the needed building blocks with photonic technologies has limited the application of this approach to usable photonic ADCs, being nowadays still in R&D stage.

Other proposed approach is based on the spatial beam steering [8]. It benefits from the advantages of using a mode-locked laser, like the photonic sampling approach and the quantization is done by spatially separated photodiodes that are focused by an optical beam depending on the signal amplitude.

D. Photonic Integrated Circuits for Photonic ADCs

Following the natural evolution of the technology for reducing the mass and size of the implementations, some relevant demonstrations of integrating functionalities in a single photonic integrated circuit (PIC) have been reported, most of them based on photonic sampling and electronic quantization. The most relevant parts of this architecture are the Mode-Locked Laser and the sampling unit. The traditional way to implement stable MLLs are by using free space of fibre laser cavities with integrated absorber that forces the pulse operation. This is a very well technology traditionally used in applications like metrology or reference generation, but limited to MHz regime. Some relevant results with fundamental frequency at GHz regime is reported in [12]. The MLL implementation in PICs is very compact but limited in jitter performance when compared with traditional MLLs. On the contrary, it is easy to achieve GHz fundamental operation. One of the most relevant results is shown in [13] where an integrated MLL in InP technology is demonstrated at frequencies as low as 4.4GHz.

Concerning the sampling section, an impressive integration exercise in Silicon Photonics have been reported in [14], in which a sampling and wavelength interleaver architecture with 4 channels is reported. This PIC was tested to sample a 10 GHz signal with 3.5 effective bits at a sample rate of 2.1 GSa/s obtained by interleaving two 1.05 GSa/s.

Table 1.
PERFORMANCES OF PHOTONIC-ADC ARCHITECTURES

Technique	Architecture	Year	Reference	ENOB (bits)	SFDR (dB)	f_s (GSps)	$f_{in\ max}$ (GHz)
Photonic Assisted ADCs	Diode Bridge T&H	2004	[3]	11.8	72	1.003	1.0073
	Time-interleaving	2004	[2]	3.5	-	-	40
	Time-Stretching	2005	[8]	-	34	-	4.7
Photonic Sampling ADCs	Pulse Demux	2003	[4]	9.8	-	0.505	-
	Integrated Pulse Demux	2011	[14]	3.5	39	2.1	10
	Pulse Demux	2014	[15]	7	70	0.4	40
	Single Channel	2007	[10]	-	40	-	10
	Single Channel	2011	[12]	9	<65	1.3	50
Photonic Sampling and Quantization ADCs	Intensity Modulator	1997	[6]	4	-	5	-
	Sigma-Delta Modulator	Do not exceed the electronic Sigma-Delta modulators performance		-	-	-	18
	Optical beam steering	2008	[7]	Since this technology is very recent, there are not experimental results yet			

Summarizing the table results, the most interesting configuration in terms of reduced complexity and improving performance is the implementation of a photonic sampling and track-and-hold placed as a front-end of a standard electronic ADC. This configuration enables an optimum sampling of the RF signal thanks to the use of a very stable optical pulsed laser, with a jitter of few femtosecond, low amplitude noise and ultra-short temporal duration (fs range). The RF signal is sampled using an electro-optical modulator, which exhibits ultra low second-order distortion (enabling the multi-octave sampling), a very low third order distortion and an infinite decoupling between the sampling and the quantification parts of the system. These characteristics enable to have a frequency independent dynamic range, optimizing the digitalization system performance and eventually overcoming the electrical ADCs and T&Hs limitations.

IV. IMPLEMENTATION OF PHOTONIC SAMPLING ADC FOR SPACE APPLICATIONS

For the current telecom payloads having a large number of feeds and thus a large number of converters the mass and consumption of the mixer stage have become significant. Moreover, the current trend in this type of satellites is the digitization of RF signals to allow for higher flexibility on the payload, thus needing the inclusion of ADCs (Analog to Digital Converter) in the payload that present new trade-offs in design (jitter, quantization noise, ambiguity). A technology development capable to solve these limitations could suppose a revolution in some satellite applications such as Satellite internet services or Full Digital TT&C service among others.

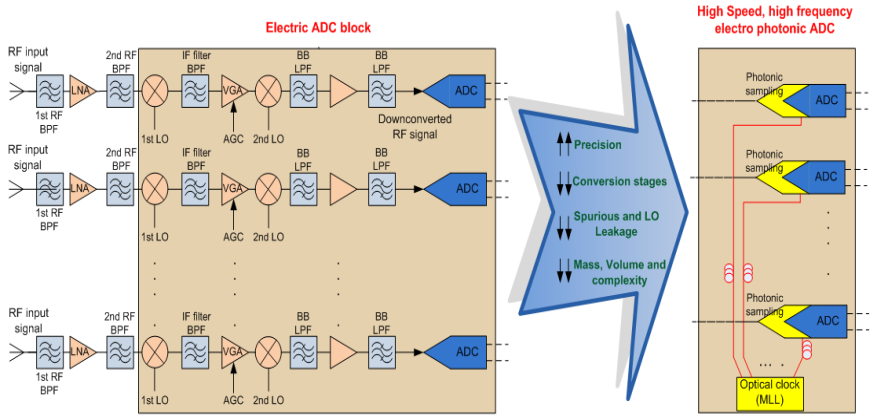

Fig. 4. General architecture of a photonic sampling ADC

Fig.4 shows the scheme of implementation of the future telecom payloads with 200-250 ADCs with the traditional solution (with LO mixer stages to carry out the frequency conversion) and the evolution with high speed, high frequency Electro-Photonic ADCs being developed in the EU FP7-PHASER project. The overall objective is to develop a space-grade, high speed digitizer capable of direct RF-sampling up to Ka band signals, exhibiting an improvement of more than two order of magnitude in the digitizer frequency response respect to the SoA, which enables a dramatic hardware complexity reduction for the next generation satellite payloads, as preliminary assessed in an ESA research program where the fundamental concept was already demonstrated with 60 dBc SFDR at Ka band [16].

Considering the commented limitations of the traditional Electronic-ADCs and taking into account the most interesting configurations of Photonic-ADCs, the architecture of the Photonic-ADC is depicted in Fig.5. Manufactured Mark I version of the Photonic subsystems is also presented as a first laboratory demonstrator of PHASER.

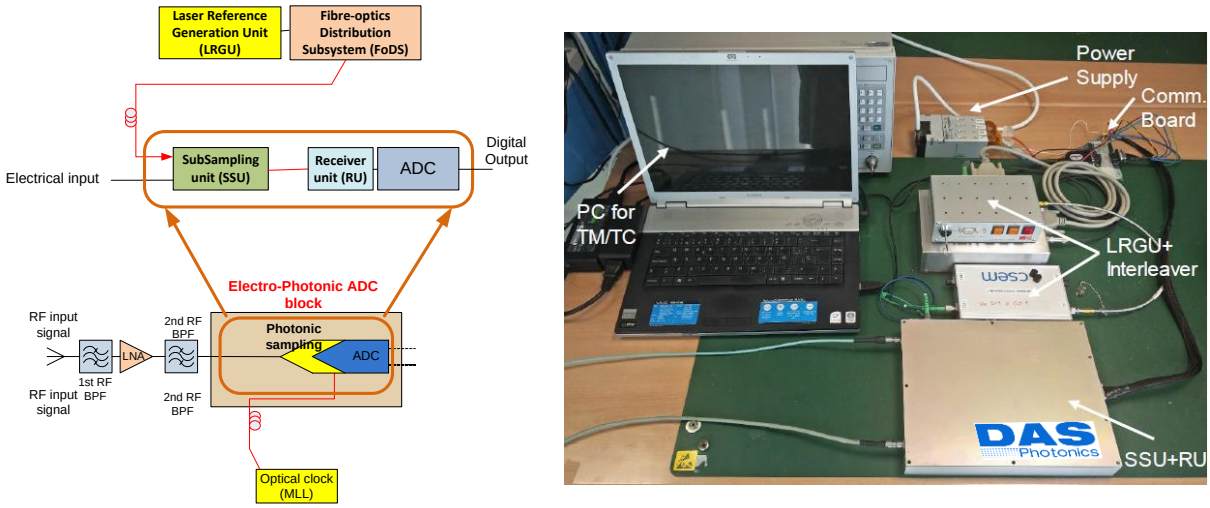

Fig. 5. Photonic-ADC architecture of PHASER (left). Mark I version of the photonic subsystems of PHASER (right)

V. MARK I TEST RESULTS

After the development of the Mark I version of the PHASER system and while the development of the Mark II (that will improve mass, volume and mechanical design of SSU, RU and ADC) is in process, different parameters have been tested in order to evaluate the performance of the system. The main results are the following:

- Input Band: S-band to Ka band
- Input full scale power: 4 dBm,
- Signal band: 500 MHz,

- Sub sampling rate: 2.636 Gsps,
- SNR@ full scale level: 55 dB,
- ENOB: 8.8 @ full scale level,
- ENOB after post processing (digital filtering @ 36 MHz): 10 bits.
- IIP3: 24.5 dBm.

Moreover, it should be noted that a very low timing jitter of 14fs in the range 1KHz - 2MHz was also achieved by the developed Mode Lock Laser that will means a high accuracy when sampling the input signal.

VI. TARGET APPLICATIONS

One target application of this technology has been identified in electronically steerable multibeam antenna (active antenna) for future communication satellites. Active antennas, also called electronically steerable antennas require a special piece of equipment: a Beam Forming Network (BFN). Among the available technologies (microwave, optical) for BFN, the digital technology is one of the most promising. Nevertheless, there is a technological bottleneck: the analog to digital conversion prior to the digital processing in every antenna element. The photonic sampling technology as the PHASER technology should be able to break free this bottleneck since the direct digitalization of the Ka or Q-V band signals can be done in the antenna, reducing the enormous number of frequency converters required in traditional implementations, especially in large Direct Radiating Array (DRA) antennas.

The second target application is digitalization of the On-board Digital Processing in the satellite allowing to perform IP Space Routing enabling to have a Standard Independent system with waveforms and coding schemes defined by software can be updated during satellite lifetime, flexible bandwidth allocation through input demultiplexer reprogramming, dynamic routing schemes through suitable programming of the routing function, ACM capabilities or dynamic resources allocation. This implementation is extremely attractive to operators due to its flexibility in the resource allocation and its evolution and lifetime capabilities.

The two previous technological applications can be mixed in a future high-power, high flexibility broadband payload that may completely revolution the way users access to satellite communication links, meaning, in practice, that each individual user or group of users would perceive the satellite as if its entire power and bandwidth were allocated exclusively to them. The proposed architecture would consist of a receiving multispot active array antenna directly digitized through a PHASER system, and then a very high performance On board Processor with Digital beamforming capabilities both in reception and transmission would feed data to a DDS system connected to an active array transmission antenna.

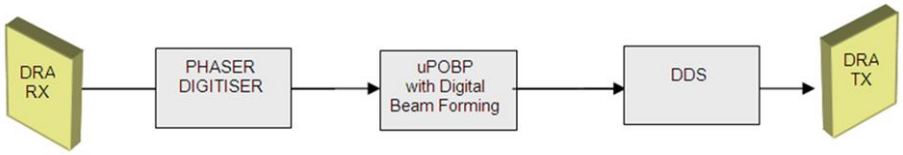

Fig. 6. Dynamic Beamforming Space Router

Taking into account that different users would access the satellite at different moments in a burst time slotted fashion, this architecture would allow associating each IP data burst to a certain antenna beamforming configuration. This means that such a system would configure the Rx and Tx ultra-narrow antenna lobes to be centered in the user position during its burst time so that during that time, the entire satellite power and antenna gains are dedicated to the users in a very narrow spot, thus allowing the satellite access to be performed with very small devices using very little RF power to obtain high bandwidth.

VII. CURRENT WORK

Fig.7 shows the Mark II version of the SSU + RU and ADC + PPAD that is being developed for the PHASER Project, in order to reduce mass, and volume and to adapt the developed Mark I version for space applications. In this way, the implemented photonic components, not only in the SSU and the RU but also in the rest of optical subsystems (LRGU and FoDS), have been tested in terms of radiation (gamma and protons) and thermal cycling, among others.

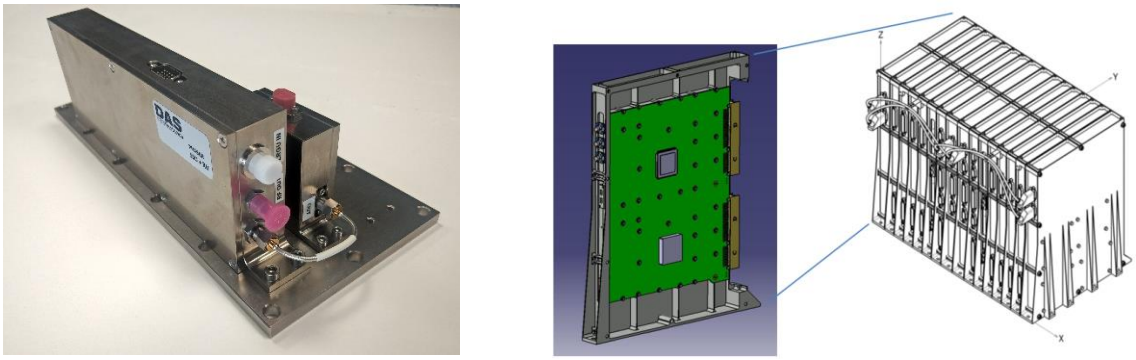

Fig. 7. PHASER (Mark II version) of SSU & RU (left) and ADC & PPAD (right)

VIII. CONCLUSION

A review of the recent developments of the photonic ADC technology have been done, paying special attention to application of receiving antenna systems. The most promising applications scenarios considered as early adopters for this technology are digital receivers in space platforms, covering digital channelizers and digital beamforming.

In this way, a Photonic-ADC suitable for its use in telecom payloads has been implemented and experimentally demonstrated in a laboratory environment (Mark I of PHASER) with TRL 5. Moreover, the development of a Mark II version of this concept with TRL 6, is in process and the product is expected to be ready to order in Q1-17.

The direct digitalization achieved with this system from Ka band to baseband makes this system as the most promising technique for applications with electronically steerable multibeam antenna (active antenna) for future communication satellites and for digitalization of the On-board Digital Processing in the satellite.

ACKNOWLEDGEMENT

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REFERENCES

[1] B. L. Shoop, "Photonic Analog-to-digital Conversion", Springer, New York, 2000.
[2] http://www.teledyne-si.com/pdf-data-converters/DS_0162PA2-3215.pdf
[3] K. Ma *et al.*, “*Low-temperature growth of GAAs on Si used for ultrafast photoconductive switches*” IEEE J. Quantum Electron. 40, 800-804 (2004).
[4] E. W. Jacobs *et al.*, “*Optically clocked track-and-hold for high-speed high-resolution analog-to-digital conversion*”, Technical Digest, 2004 IEEE International Topical Meeting on Microwave Photonics, 190-192 (2004).
[5] R. C. Williamson *et al.*, “*Precision calibration of an optically sampled analog-to-digital converter*”, *Digest of IEEE LEOS Summer Topical Meeting on Photonic Time/Frequency Measurement and Control*, 22-23 (2003)
[6] M. Johansson, B. Lofving, et al., U. Westergren and C. Pala, “Study of an ultrafast analog-to-digital conversion scheme based on diffractive optics,” *Appl. Opt 39*, 2881-2887 (2000).
[7] P. P. Ho, Q. Z. Wang, et al., “Ultrafast optical pulse digitalization with unary spectrally encoded cross-phase modulation,” *Appl. Opt. 36*, 3425-3429 (1997).
[8] M. Jarrahi, R. Fabian, W. Pease, T.H. Lee, “Spatial Quantized Analog-to-Digital Conversion Based on Optical Beam-Steering,” *Journal of Lightwave Technology*, vol. 26, no. 14, july 15, 2008
[9] Y. Han and B. Jalali, “Continuous-time time-stretched analog-to-digital converter array implemented using virtual time gating,” *IEEE Trans. Circuits and Syst.* – I 52, 1502-1507 (2005).
[10] J. A. Bell *et al.*, “Extension of electronic A/D converters to multi-gigahertz sampling rates using optical sampling and demultiplexing techniques,” *23rd Asilomar Conf. on Signals, Systems and Computers*, ed. R. R. Chen, 1, 289-293 (1989).
[11] G. McDonald, J. Cooper, R. Wilson, “*Opto-electronic digitisation techniques for ultra-wideband signal capture*”, QinetiQ presentation in Workshop on “Optoelectronic Technologies and Priorities”, London, October 17th-18th 2007
[12] M.A. Piqueras, P. Villalba, J. Puche and J. Martí, "*High Performance Photonic ADC for Space and Defence Applications*", IEEE COMCAS, Tel-Aviv 2011.

[13] Mickaël Faugeron *et al.,"High Peak Power, Narrow RF Linewidth Asymmetrical Cladding Quantum-Dash Mode-Locked Lasers"*, IEEE JSTQE, VOL. 19, NO. 4, JULY/AUGUST 2013
[14] Anatol Khilo *et al.," Photonic ADC: overcoming the bottleneck of electronic jitter"*, OPTICS EXPRESS, Vol. 20, No. 4, pp. 4454-4469, 13 February
[15] Paolo Ghelfi *et al., " A fully photonics-based coherent radar system"*, Nature **507**, 341–345 (20 March 2014)
[16] ESA contract "*Electro-Photonic ADC*", T516-017MM