Towards 3nm overlay and critical dimension uniformity: an integrated error budget for double patterning lithography

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ABSTRACT

Double patterning has emerged as the likely lithography technology to bridge the gap between water-based ArF immersion lithography and EUV. The adoption of double patterning is driven by the accelerated timing of the introduction of device shrinks below 40nm half pitch, especially for NAND flash. With scaling, increased device sensitivity to parameter variations puts extreme pressure on controlling overlay and critical dimension uniformity. Double patterning also makes unique demands on overlay and CDU. Realizing that there is no further increase in NA past the current 1.35 on the horizon, the focus has shifted from a straight shrink using the newest tool to learning how to reduce the effective k_1 through improvements to the tool's control of CDU and overlay, as well as innovative RET, mask, and process technology.

In double patterning lithography, CDU and overlay are complex and entangled errors. In an approach where the pattern is split into two masks and recombined in successive lithography and etch steps, a line or space width is defined by edges placed at separate masks. In an approach where double patterning is achieved by self-aligned processes, CD error at the first sacrificial mask will translate into pattern placement errors in the final pattern. In all approaches, it is crucial to understand how these errors interact so that the combined effects can be minimized through proper tool controls, mask OPC and split algorithms, and process choices. Without aggressive actions, the complexity of this problem combined with the economic drawbacks of using multiple masking steps to define critical device layers threaten to slow overall device shrink rates.

This paper will explore the main sources of critical dimension and overlay errors in double patterning lithography and will point out directions we may follow to make this an effective manufacturing solution.

1. Introduction

The adoption of double patterning is driven by the accelerated timing of the introduction of device shrinks below 40nm half pitch, especially for NAND flash. This has resulted from differences in the layout of various devices, as was reported last year (1). With scaling, increased device sensitivity to parameter variations puts extreme pressure on controlling overlay and critical dimension uniformity. Double patterning also makes unique demands on overlay and CDU. This paper explores the combined issues of scaling and double patterning as they affect overlay and CDU.

In section 2, CDU requirements for advanced logic and memory devices will be discussed. Error budgets for one dimensional dense and isolated lines will be explored. In the future more complex two dimensional geometries will be treated. Overlay requirements and error budgets will be reviewed. In combination with CDU requirements it is possible to outline the highlights of design rule setting for common problems such as contact to gate spacing in a 6T SRAM, or wordline to contact spacing in a NAND flash device.

In section 3, the error budgets for two different double patterning approaches are outlined: for Litho-Etch-Litho-Etch (LELE), and for spacer, or self-aligned, double patterning.

In section 4, methods to minimize final CDU and overlay errors using active compensation of dose and edge placement are reviewed.

2.   Critical Dimension Uniformity and Overlay Requirements for CMOS Logic and Memory-Single Exposure

Critical dimension uniformity (CDU) in optical lithography has been studied for single exposures many times (2). The problem of how to characterize CDU over a wide range of feature types which have optical proximity corrections applied has also become a topic of interest (3). Likewise, the interplay of CDU and overlay errors have long been the subject of study in order to develop design rules which minimize cell area but maximize device yields (4).

In a single exposure step, a pattern is created at once from correlated edges and CDU is based on pattern control. Design rules are defined by placement control of edges generated in separate process steps (layers). Edge placement from one layer is uncorrelated to edge placement from the following layer. CDU for a single exposure is illustrated in Figure 1. A mask with dense and isolated lines is shown. At lithography, the dense lines are printed to $L_{dense\ litho}$ while the isolated line is printed to $L_{iso\ litho}$. After etch, the dense lines are $L_{dense\ etch}$ while the isolated line is $L_{iso\ etch.}$ Due to proximity effects in lithography as well as etch loading effects, L_{dense} and L_{iso} are usually not equal. Mask bias is usually applied to bring these widths in line. Inside the dense array, every line is usually equal in width except for small variations due to the mask or line edge roughness. Likewise spaces are equal in width.
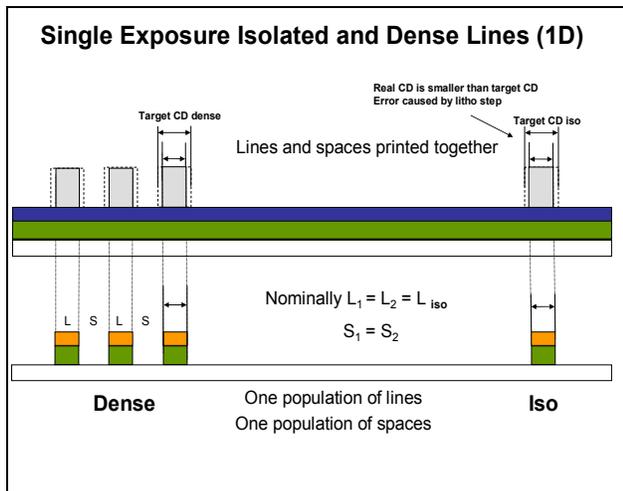
Figure 1: Single Exposure Lithography Requirements (1D)
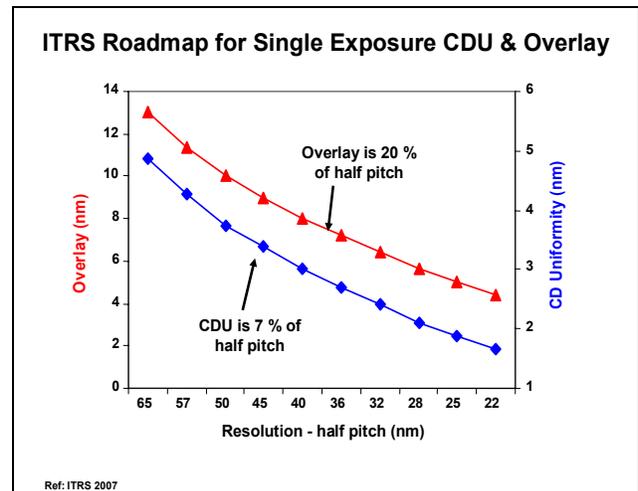
Figure 2: ITRS Roadmap for Single Exposure CDU and Overlay

The ITRS roadmap for single exposure CDU allocates 7% of the half pitch to lithography, while overlay of critical layers is expected to be 20% (Figure 2). For technology node below 40nm, evolution of CDU and Overlay shown in Fig 2 assumes a hypothetical Single Exposure technique, or implies EUV.
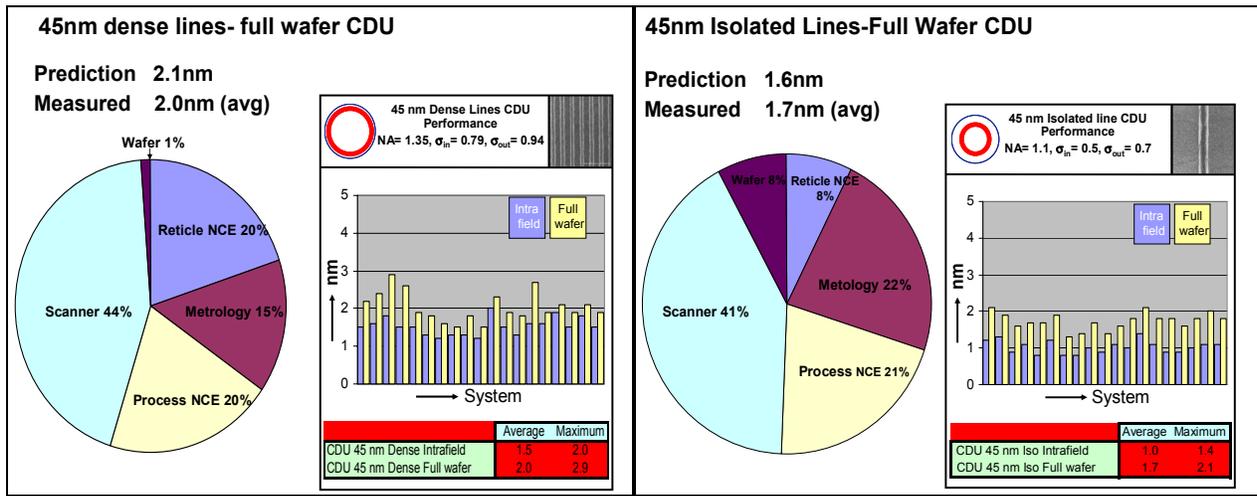
Figure 3: 45nm Dense Lines- Full Wafer CDU

Figure 4: 45nm Isolated Lines-Full Wafer CDU

Figures 3 and 4 show average intrafield and full wafer CDU data for 45nm dense and isolated lines printed on 20 XT1900Gi immersion scanners. The NA and illumination conditions were chosen to demonstrate the best tool performance: NA 1.35, annular 0.94/0.79 for the dense lines, and NA 1.1, annular 0.7/0.5 for the isolated lines. Reticle and systematic resist process errors are removed from the data to indicate the magnitude of the non-correctable errors. Predictions of the CDU based on error budgets for principal components of error such as dose, focus, MSD, etc. match well with the measured data, indicating a good understanding of the main error sources. See (5) for a discussion of how the CDU is calculated and experimental conditions for this data.

Improving overlay for double patterning is a strong imperative. Current tool overlay budgets for immersion scanners are about 6nm (6), with clear directions how to reduce to less than 4 and 3nm through improvements in optics, positioning, and thermal and mechanical control (see Figure 5). Furthermore, there are substantial errors induced by processing and by reticles. These errors can be partly compensated with higher order grid corrections (see Figure 6). In this experiment, standard CMOS front end processing was used, and overlay of gate to active was measured (XT1700i, NA 1.2).
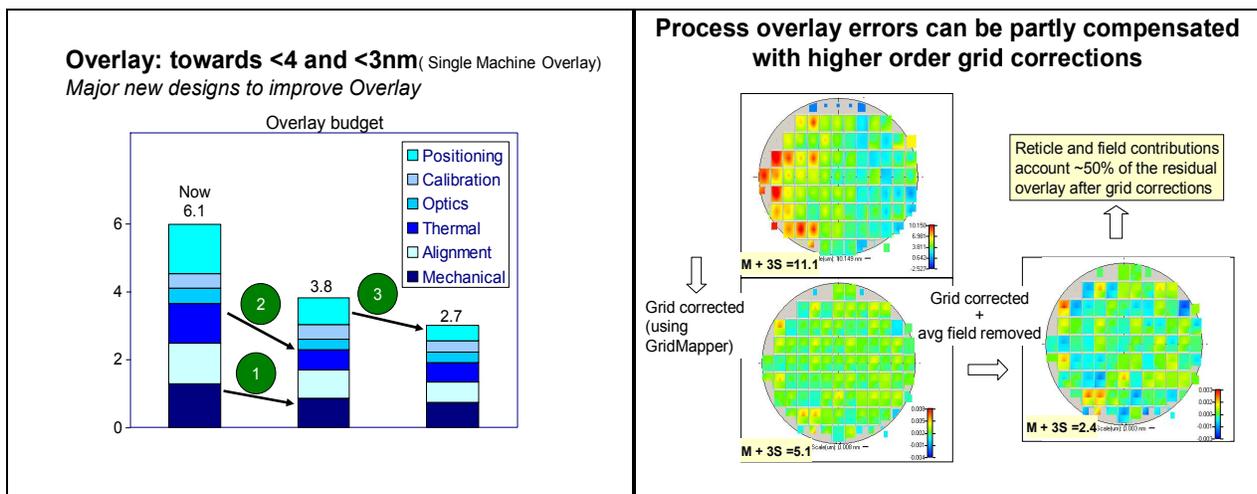
Figure 5: Overlay: towards<4 and <3nm (Single Machine Overlay)

Figure 6: Process overlay errors can be partly compensated with higher order gird corrections

3. Entangled CDU and Overlay requirements for double patterning

To recap, for single exposure, a pattern is created at once from correlated edges and CDU is based on pattern control. Design rules are based on placement control of edges generated in separate process steps (layers). Layer-to-layer edge placement are uncorrelated. The classical problem of determining the minimum spacing between contact and gate in CMOS devices of many varieties is illustrated in Figure 7. The CDU and overlay errors for a single exposure at 32nm half pitch are estimated in Figure 8 using estimates for component errors which are added in quadrature.

Entangled CD & Overlay control for Design Rule decision

What is the minimum Contact to Gate edge-to-edge separation supported by a technology node?

$X_{MIN\_wafer} > a$

Where the a parameter is set by device reliability requirements to avoid shorts failures

$$X_{NOM\_wafer} = X_{design} + \tfrac{1}{2} Gate_{shrink} - \tfrac{1}{2} Contact_{increase}$$

$$X_{MIN\_wafer} = X_{NOM\_wafer} - Tol$$

$$Tol = \tfrac{4}{3}\sqrt{\left(\tfrac{3}{2}\sigma_{CH-CD}\right)^2 + \left(\tfrac{3}{2}\sigma_{Gate-CD}\right)^2 + \left(3\sigma_{OL\_Gate-to-CH}\right)^2}$$

$$X_{design} > a - \tfrac{1}{2} Gate_{CDshrink} + \tfrac{1}{2} CH_{CDincrease} + \tfrac{4}{3}\sqrt{\left(\tfrac{3}{2}\sigma_{CHCD}\right)^2 + \left(\tfrac{3}{2}\sigma_{GateCD}\right)^2 + \left(3\sigma_{OL\_Gate-to-CH}\right)^2}$$

Single exposure CDU + OL budget at 32nm *for reference*

Figure 7: Entangled CD & Overlay control for DR decision

Figure 8: Single exposure CDU and OL budget at 32nm

In double patterning, a pattern is created from two separated and generally, uncorrelated edges and the CDU should be based on edge control. Design rules should be defined by placement control of edges generated on the same DPL-created layer which has been created from separate process steps (layers). Layer-to-layer edge placement errors are uncorrelated. Twice as many edge placement errors are required for design rule decisions.

Double patterning options, Spacer and LELE, can be either a "positive" or a "negative" process flow (1). In this paper, we consider only the positive LELE and spacer processes.

A simple process flow for LELE is shown in Figure 9. Due to lithography and etch variations from target at both masks, and due to the overlay error between mask 1 and mask 2, we have in the end four CD populations, two for lines L1 and L2, and two for spaces, S1 and S2. The two line-CD populations are generally uncorrelated and deviate from each other in their mean-CD, statistical and spatial distributions. Space-CD populations are generally correlated through the overlay error, but are uncorrelated from line-CD populations. An estimated budget for LELE at 32nm half pitch is shown in Figure 10 (reference 7 indicates how these budgets are calculated using straightforward error statistics for treating two separate populations).
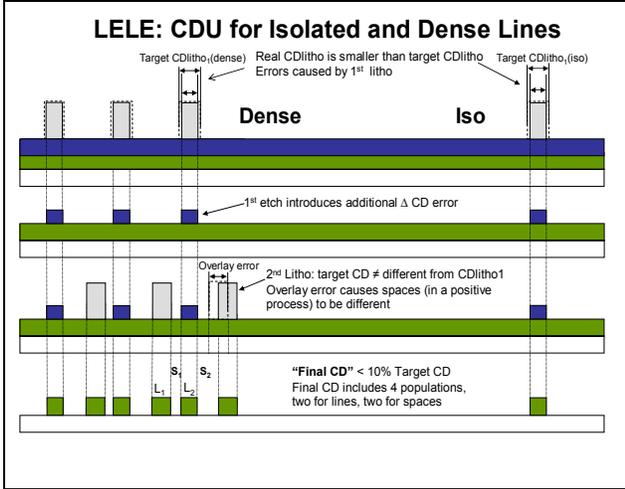
Figure 9: LELE:CDU for Isolated and Dense Lines
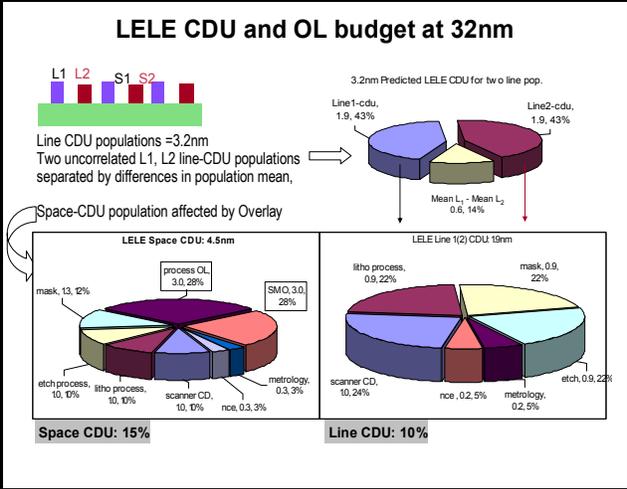
Figure 10: LELE DPL CDU and OL budget at 32nm

Experiments were performed (8) for a full LELE process at 32nm half pitch using a 1.2NA immersion scanner (XT:1700i) for both lithography steps. The results for mean target error between L1 and L2, and S1 and S2, and for CDU were remarkably close to the predictions, as shown in Figure 11 for lines, and in Figure 12 for the spaces.
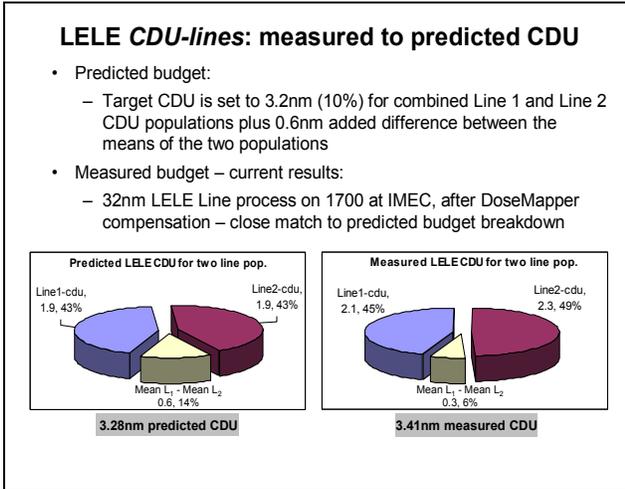
Figure 11: LELE CDU lines: measured to predicted CDU

LELE *CDU-space*: measured to predicted CDU

- Predicted budget:
  - Target CDU-space is set to 4.5nm (15%) and includes space CDU combined with overlay error
- Measured budget:
  - 32nm LELE process on 1700 at IMEC; after DoseMapper
  - Measured overlay of ~ 3.3nm including SMO and process

	Predicted (nm)	Measured (nm)
Scanner (imaging) and patterning	1.7	2.2
Overlay (SMO, process)	4.2	3.3
Reticle	1.3	1.5
Others	0.4	?
Total	4.8nm	5.6 measured
		3.8nm after DoseMapper corrections

Overlay entangled in CDU

Figure 12: LELE CDU-space: measured to predicted CDU

In an approach where double patterning is achieved by self-aligned, or spacer, processes, CD error at the first sacrificial mask will translate into pattern placement errors in the final pattern. This is illustrated in Figure 13. Here lines L1 and L2 are highly correlated and can have comparatively small variation due to the fine control possible in film deposition and planarization. However, spaces S1 and S2 can vary widely mostly driven by targeting errors in the first sacrificial lithography step. Thus the CDU requirement for this first mask is the most critical in the spacer process. Errors in the

sacrificial layer end up looking like local overlay errors in the final pattern, a phenomenon known as pitchwalking. A budget for spacer patterning at 32nm half pitch is estimated in Figure 14.
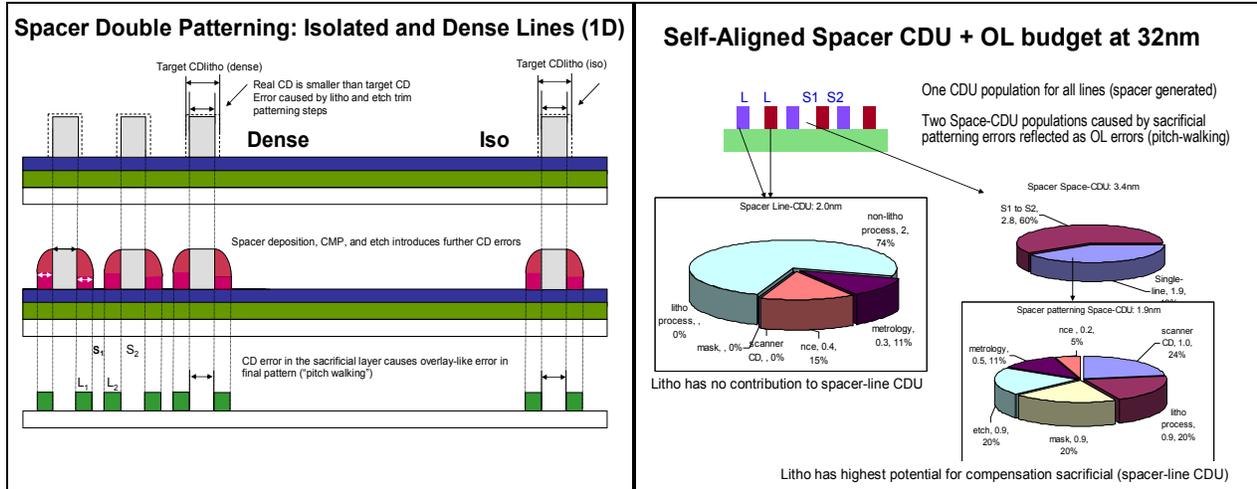
Figure 13: Spacer Double Patterning Litho requirements   Figure 14: Self-aligned CDU + OL budget at 32nm

In spacer patterning we have in the end three CD populations, two for space S1 and S2, and one for lines. In reality, there are also two line-CD populations, but because of the spacer deposition uniformity and conformity, the line-CD populations are extremely well correlated and have almost identical Mean-CD. The two space-CD populations are generally uncorrelated and deviate from each other in their mean-CD, statistical and spatial distributions.

4.   Improvement paths for double patterning

Here we offer three critical directions for improvement in double patterning: mask, active dose compensation (DoseMapper), and active grid compensation (GridMapper). The usefulness of GridMapper was previously discussed (1, Figure 6).

The mask contributes 20 to 25% of wafer CDU and overlay errors, and since two masks are always required in double patterning, this is a key component to understand and improve. In a single exposure, CDU and overlay are equally important, and the roadmap to control it is well understood for 32nm: CDU of ~6nm, overlay of ~8nm at reticle level. In LELE, the overlay, target CD, spatial correlations of CDU and registration maps are critical. Requirements are approximately CDU of ~4nm; overlay of ~5nm; and correlation of spatial maps > 80%. In spacer, the challenge is to control local variation in CDU and registration, with requirements: CDU of ~4nm, registration of ~4nm.

Writer, blank, process, and metrology tool all contribute to the registration budget of the mask. The key challenge is improving writer local placement accuracy. For blank contributions: charging, heating, and relieved stress. For writer contributions: stage drift and tracking => sequential writing. For pellicle contributions: mounting-induced stress. Finally, the metrology tool contributions must be driven to sub-nm levels. A potential new requirement is dedication of writer and process for producing each pair of double patterning reticles.

Current best mask CDU performance for double patterning reticles is shown in Figure 15. CDU of less than 3.5nm is demonstrated on both plates and the spatial signature of each is very well correlated. In Figure 16, the strong correlation of mask to wafer overlay data for these masks is shown (9, 10).

CD Performance: CDU spatial map on DPL patterns

CD performance of DPL features

Layer	Off-target (nm)	CDU (nm,3σ)
1	1.3	3.0
2	1.6	3.3

Matching of CDU Signatures

Correlation Coefficient	Max Deviation (nm)
0.86	1.9

• Promising off-target performance with negligible mean-to-target difference
• Similar CDU signature on both masks

Bubke, et. al., SPIE Photomask 2007
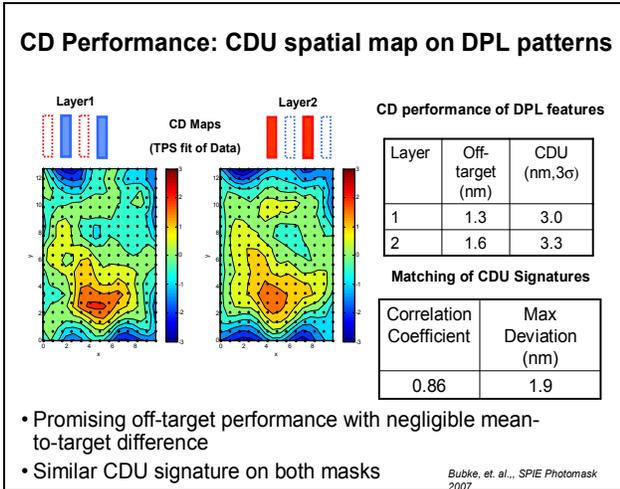
Figure 15: CD Performance: CDU spatial map on DPL patterns

Correlation Reticle vs Wafer Overlay

Mask-1 to mask-2 Overlay (calculated from mask 1 and 2 registration)

X cor.

Corresponding layer-1 to layer-2 wafer Overlay

Y cor.

Overlay signature from Mask1 to Mask2 clearly transfers onto Layer-1 to Layer-2 wafer overlay signature

R.deKruif, et. al., EMLC Photomask 2008
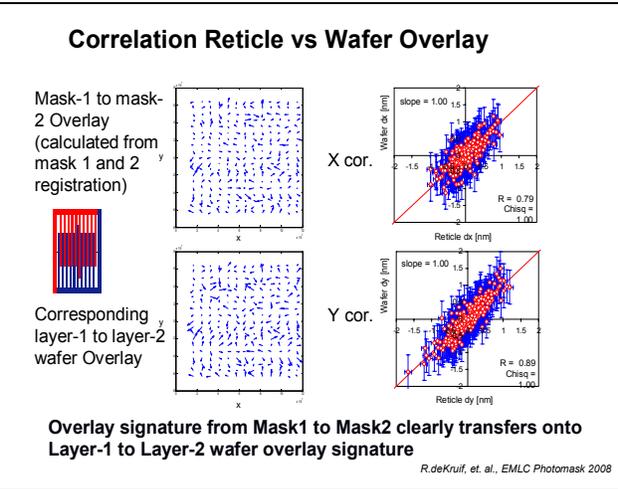
Figure 16: Correlation Reticle vs Wafer Overlay

Exposure-related CD control for wafer CDU concerns are as follows. For a single exposure, one wants to minimize intra (incl. reticle)/interfield CDU. For LELE, we want to bring together two CD populations, minimize the difference between populations mean, both intra- and interfield. The reticle and intrafield CDU is more critical. We wish to match the CDU fingerprint maps of two populations, intra/interfield, and to distinguish patterns (1st or 2nd). For spacer, we require extreme control and compensation of sacrificial patterning. This means emphasis on extreme control over 1st pattern CDU (+Mean to target), both litho and etch performance. Then we need to minimize the CD difference between 1st and 2nd patterning.

Interfield DoseMapper for LELE lines CDU control

• Goal: bring LELE interfield line CDU to calculated tolerances for variance and mean difference (for 32nm)
  – CDU variance/population: <2nm; difference between means: <0.8nm

	Line1 (3s)	Line2 (3s)
Before DoseMapper	4.6nm	5.5nm
After DoseMapper	2.1nm	2.3nm
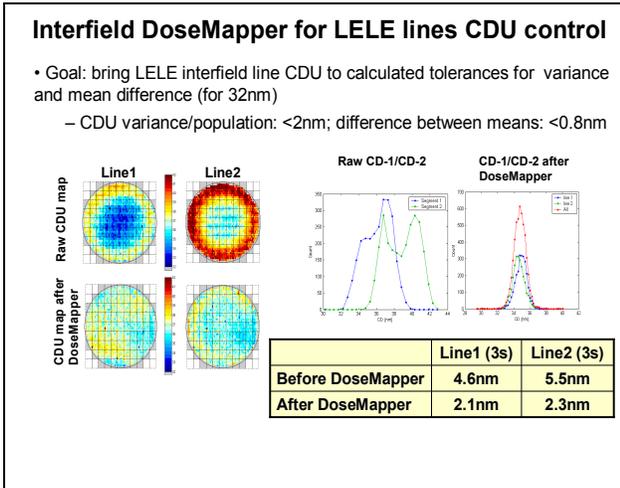
Figure 17: Interfield DoseMapper for LELE lines CDU control

32nm Spacer Final result (experimental data: CD-SEM)

Line1 Mean=32.7 3σ=2.1nm
Line2 Mean=32.7 3σ=2.0nm
Space1 Mean= 30.0 3σ=2.1nm
Space2 Mean=32.8 3σ=4.1nm

Expected performance after applying DoseMapper (calculated)

Line1 Mean=32.7 3σ=2.1nm
Line2 Mean=32.7 3σ=2.0nm
Space 1 Mean= 31.3 3σ=2.3nm
Space 2 Mean= 31.3 3σ=2.8nm
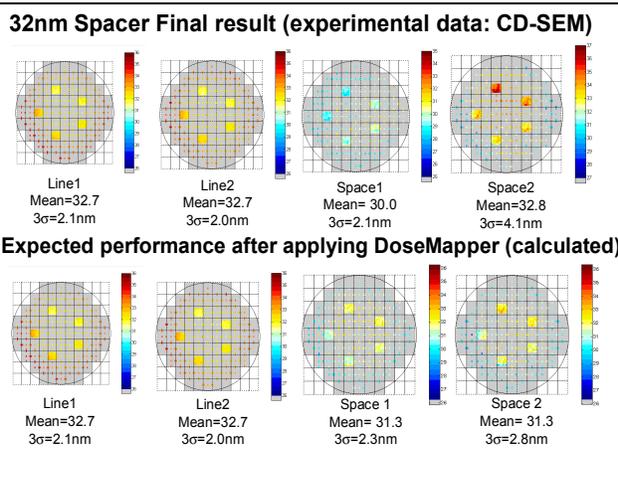
Figure 18: 32nm Spacer Final result (experimental data: CD-SEM)

The use of active dose compensation for LELE is illustrated in Figure 17 (8) in which the distributions of L1 and L2 as well as the mean to target error are substantially reduced. Likewise, active dose compensation in a spacer process can be used to bring the two space widths S1 and S2 much closer together (Figure 18). Simple calculations as illustrated in

Figure 19 indicate the CD control of the sacrificial layer in a spacer process must be of order 4X tighter than in a single exposure, as is borne out through experiment.

A summary of budget predictions and corresponding experimental results for 32nm half pitch LELE and spacer processes are given in Figure 20.

Spacer needs tighter CD control

Sacrificial pattern width variation caused by Litho + HD etch

Experimentally measured sensitivity to changes in exposure dose for spacer process

ε: positional change of one edge

$$\left. \begin{array}{l} S_1' = S_1 - 2\varepsilon \\ S_2' = S_2 + 2\varepsilon \end{array} \right\} \Delta S = 4\varepsilon$$

Pattern	Normalized Sensitivity nm/mj
Hardmask	a
S1	1.8a
S2	-2a
S1-S2	-3.7a

To control pitch-walking, CD control of sacrificial pattern should be ~4x tighter than SE

All DPL: measured CDU before/after corrections

- 32nm LELE and Spacer baseline processes on 1700 at IMEC
- Encouraging results towards achieving 3nm CDU and OL control for DPL
  - Litho compensation of inter and and intrafield processing variation is unavoidable to reach 3nm control tolerances

	Expected CDU (nm)	measured LELE	LELE +Litho compensations experimental	measured Spacer	Spacer+ Litho compensation modeled
CDU Line 1	1.9	4.6	2.1	2.1nm	2.1nm
CDU Line 2	1.9	5.5	2.3	2.1nm	2.1nm
Line1-Line2 mean difference	0.6	2.5	0.3		
Overlay	3	2.5 to 3.6	3		
CDU space 1	4.8	5.7	3.7	2.1nm	3.3nm
CDU space 2		5.6	3.8	4.1nm	2.9nm
Space1-Space2 mean difference	< 1			2.8nm	0.2nm

Overlay entangled in CDU

CDU entangled in local overlay

Figure 19: Spacer needs tighter CD control   *Figure 20: All DPL: measured CDU before/after corrections*
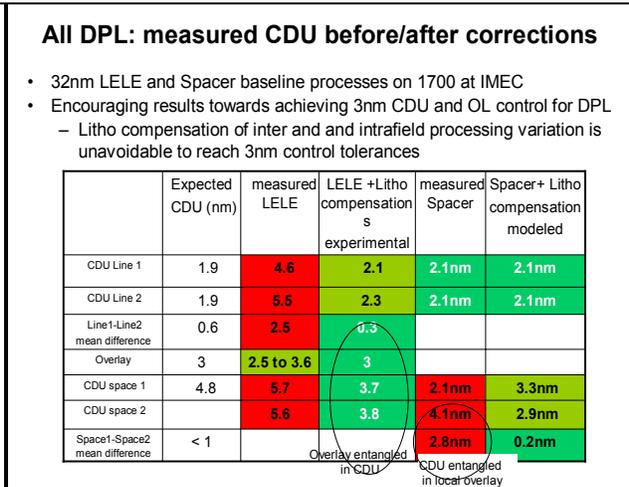
5.   Conclusions

Double exposure and double patterning solutions are being pursued to reduce effective k_1 below 0.3, and with required overlay and productivity. This is the only technology available for volume manufacturing in the 2008-11 timeframe. Realistic error budgets indicate double patterning is limited to about 25nm half pitch for complex IC patterns.

New challenges include the entanglement of CD and overlay errors and the need to distinguish the different populations. In considering the extension of 193nm lithography to 3X and 2X nodes, we realize there is no new NA on the horizon, so the focus shifts from a straight shrink to learning how to reduce the effective k1 through double patterning. Spacer and LELE are the most likely approaches. LELE is a lower cost, higher productivity opportunity. Spacer can be used with any existing lithography tool but is more complex to layout and process. The implications for the litho tool are profound. Both spacer and LELE require much tighter CDU than required from SE lithography; LELE must also achieve overlay on the order 3nm. It is currently thought that < 1nm CD and < 2.5nm OL controls become unrealistic and expensive. Tighter CDU and overlay budgets should be achieved through active compensation of wafer and field spatial distributions.

6.   Acknowledgements

7.   References

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