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# All-optical logic gates based on nanoring insulator–metal–insulator plasmonic waveguides at optical communications band

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**Abstract.** We propose, analyze, and simulate a configuration to realize all-optical logic gates based on nanoring insulator–metal–insulator (IMI) plasmonic waveguides. The proposed plasmonic logic gates are numerically analyzed by finite element method. The analyzed gates are NOT, OR, AND, NOR, NAND, XOR, and XNOR. The operation principle of these gates is based on the constructive and destructive interferences between the input signal(s) and the control signal. The suggested value of transmission threshold between logic 0 and logic 1 states is 0.25. The suggested value of the transmission threshold achieves all seven plasmonic logic gates in one structure. We use the same structure with the same dimensions at 1550-nm wavelength for all proposed plasmonic logic gates. Although we realize seven gates, in some cases, the transmission of the proposed plasmonic logic gates exceeds 100%, for example, in OR gate (175%), in NAND gate (112.3%), and in XNOR gate (175%). As a result, the transmission threshold value measures the performance of the proposed plasmonic logic gates. Furthermore, the proposed structure is designed with a very small area (400 nm × 400 nm). The proposed all-optical logic gates structure significantly contributes to the photonic integrated circuits construction and all-optical signal processing nanocircuits. © The Authors. Published by SPIE under a Creative Commons Attribution 4.0 Unported License. Distribution or reproduction of this work in whole or in part requires full attribution of the original publication, including its DOI. [DOI: [10.1117/1.JNP.13.016009](https://doi.org/10.1117/1.JNP.13.016009)]

**Keywords:** optical logic gates; insulator–metal–insulator plasmonic waveguides; surface plasmon polaritons.

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## 1 Introduction

All-optical devices based on surface plasmon polaritons (SPPs) have been the topic of comprehensive research in recent years. All-optical SPP devices have extensively motivated new actions to overcome the major performance constraints of semiconductor electronic devices, which suffer from ingrained delay and high-heat generation, and to overcome the problem of photonics devices, that is, the diffraction limit. Therefore, the utilization of the aforementioned devices enabled the manipulation of light on a subwavelength scale.<sup>1</sup> SPPs are the interaction of electromagnetic waves and the free electrons of metals, propagating on the metal–dielectric or dielectric–metal interfaces.<sup>2,3</sup> Different passive and active plasmonic devices, such as nanocavities,<sup>4</sup> Bragg reflectors,<sup>4</sup> splitters,<sup>5</sup> resonators,<sup>6</sup> couplers,<sup>7</sup> modulators,<sup>8</sup> multi/demultiplexers,<sup>9</sup> stub waveguides,<sup>5</sup> hybrid plasmonic waveguides,<sup>10</sup> switches,<sup>11,12</sup> and logic gates,<sup>13–18</sup> have been realized so far. On the subject of all-optical logic gates, several studies have been proposed, analyzed, and investigated, for example, single semiconductor optical amplifiers,<sup>19</sup> hybrid plasmonic-photonic crystal nanobeam cavities,<sup>18</sup> two-photon absorption in silicon waveguides,<sup>20</sup> silicon microring resonators,<sup>21,22</sup> cross-phase modulation,<sup>23</sup> and nanophotonic plasmonics.<sup>24</sup>

Recently, many all-optical plasmonic structures provided nanoscale logic gates.<sup>25–29</sup> Each nanologic gate has a different way to realize the functions of the gates, a different number

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of logic gates, different types of logic gates, different values of resonance frequencies, different geometries, different materials of the structure, and different values of transmission.

In this paper, we offer the largest number of plasmonic logic gates (seven) in the same structure with the same resonance frequency and the same transmission threshold in structure with nanoring resonator and plasmonic nanowaveguides. The plasmonic logic gates that are proposed, analyzed, and realized are NOT, OR, AND, NOR, NAND, XOR, and XNOR. The simulation results are obtained by finite element method (FEM). In future, these devices will be the gateway to the nanophotonic-integrated circuit applications.

The organization of this paper is as follows: Sec. 2 contains the proposed structure layout and theoretical operation concept. In Sec. 3, the simulation results and performance of the proposed all-optical plasmonic logic gates are presented, demonstrated, and discussed. In Sec. 4, a comparison between the proposed work and the previous researches is introduced. Finally, we conclude the suggested work in Sec. 5.

## 2 Structure Layout and Theoretical Concept

The proposed structure which realizes the seven all-optical plasmonic gates is shown in Fig. 1.

The structure consists of three straight stripes and two nanoring resonators to construct seven logic gates based on the insulator–metal–insulator (IMI) plasmonic waveguides. The dimensions of the proposed structure are  $400 \times 400$  nm, and the length of the middle and side stripes ( $L_s$ ) are 400 and 250 nm, respectively. The width ( $w$ ) of these stripes is 20 nm, the radii of the nanoring resonator (a) and (b) are 25 and 50 nm, respectively, and the coupling distance ( $d$ ) between the nanoring resonator and the stripes is 7.5 nm.

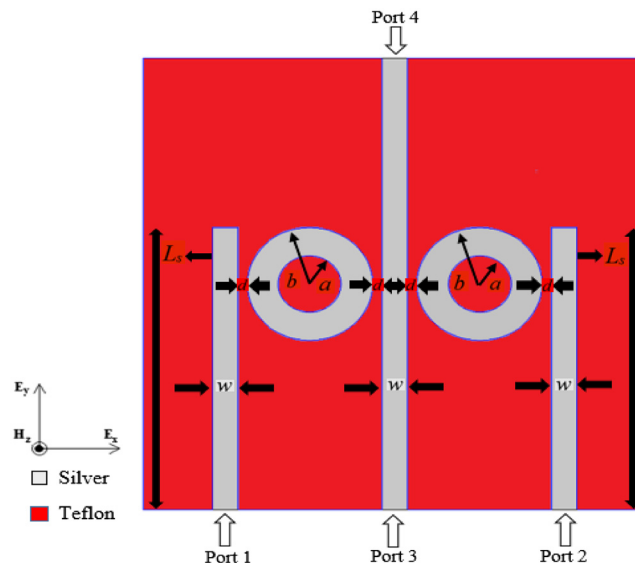
In our structure, we choose the IMI plasmonic waveguides instead of the metal–insulator–metal (MIM) plasmonic waveguides due to the advantages of IMI over MIM, according to the summarized comparison between IMI and MIM in Table 1.

In addition to the above comparison, the MIM plasmonic waveguide becomes inefficient to use as logic gates in dimensions  $< 50$  nm (width of middle material).<sup>30</sup>

The materials of the proposed structure are silver and Teflon. In our structure, stripes and two nanorings are represented as silver material, and the remaining part of the structure is a Teflon material as shown in Fig. 1.

All seven proposed plasmonic logic gates have the same dimensions, parameters, and materials in their structures.

In our simulations, Johnson and Christy<sup>42</sup> data are used to describe the silver permittivity, and the refractive index of Teflon material is 1.375.<sup>43</sup> The resonance wavelength of the nanoring can be determined by Refs. 40 and 44:



**Fig. 1** The proposed structure for the proposed plasmonic seven logic gates.

**Table 1** Comparison between IMI plasmonic waveguides and MIM plasmonic waveguides.

| Sr. No.                  | IMI plasmonic waveguides | MIM plasmonic waveguides |
|--------------------------|--------------------------|--------------------------|
| 1 <sup>30–40</sup>       | More propagation length  | Less propagation length  |
| 2 <sup>30–40</sup>       | Less confinement         | More confinement         |
| 3 <sup>30–40</sup>       | Less propagation loss    | More propagation loss    |
| 4 <sup>31,33,37,39</sup> | More quality factor      | Less quality factor      |
| 5 <sup>31,33,35,39</sup> | More figure of merit     | Less figure of merit     |
| 6 <sup>41</sup>          | Easy fabrication         | Fabrication is not easy  |
| 7 <sup>41</sup>          | Low coupling loss        | More coupling loss       |

$$\lambda_{\text{sp}} = 4\pi n_{\text{eff}} D, \quad (1)$$

where  $n_{\text{eff}}$  is the effective refractive index and  $D$  is the bigger diameter of the nanoring. According to Eq. (1), the structure parameters and the type of materials play a role in choosing the resonance wavelength. We focus on the resonance wavelength of 1550 nm, as this wavelength is the best choice in optical communications applications.

The dispersion relation equation for transverse magnetic (TM) mode in the waveguide is given by Refs. 40 and 45:

$$\varepsilon_m k_d + \varepsilon_d k_m \tan h\left(\frac{k_m}{2} w\right) = 0, \quad (2)$$

where  $\varepsilon_d$  is a dielectric constant of the insulator,  $\varepsilon_m$  is a dielectric constant of the metal, and  $w$  is thin metal thickness:

$$k_d = (\beta^2 + \varepsilon_d k_0^2)^{1/2} \quad (\text{dielectric wave number}), \quad (3)$$

$$k_m = (\beta^2 + \varepsilon_m k_0^2)^{1/2} \quad (\text{metal wave number}), \quad (4)$$

$$k_0 = 2\pi/\lambda \quad (\text{free space wave number}), \quad (5)$$

where  $\beta$  is the propagation constant that is represented by an effective refractive index of the waveguide for SPP, such as depicted in

$$n_{\text{eff}} = \beta/k_0. \quad (6)$$

Maxwell equations are solved numerically using the two-dimensional (2-D) FEM method; we have used a convolutional perfectly matched layer (CPML) as the absorbing boundary condition of the area under simulation. The structure is excited by a TM-polarized plane wave with electromagnetic field components of  $E_x$ ,  $E_y$ , and  $H_z$ .

The proposed structure has four ports, namely the two input ports, control port, and an output port. These ports are decided according to the required plasmonic logic gate. The SPPs are excited with launching a TM-polarized plane wave to the input port(s) and control port. The performance of the seven plasmonic logic gates is measured by two criteria: the first is the transmission of the optical power from the input port(s) and the control port to the output port as a function of wavelength. This can be done by choosing a threshold value of transmission between logic 1 (ON state) and logic 0 (OFF state) at the output in order to decide the type of states (ON or OFF); the value of transmission threshold has been chosen as 0.25 in order to achieve the seven plasmonic logic gates in the same structure.<sup>46</sup> The second criterion is the contrast or an extinction ratio between optical power or transmission of the ON and OFF states of the output port, whenever the variance between the optical output power or the transmission of these states is large, the performance of the plasmonic logic gate becomes better. These two criteria are described by

Eqs. (7)<sup>26</sup> and (8),<sup>28</sup> respectively. In our proposed plasmonic logic gates, we are depending on the transmission threshold to decide the desired logic gate:

$$T = P_{\text{out}}/P_{\text{in}} \quad (\text{for ON and OFF states of the output port}), \quad (7)$$

where  $T$  is the transmission,  $P_{\text{out}}$  is the output optical power of the output port in ON state and OFF state, and  $P_{\text{in}}$  is the input optical power to the input port (s) and control port. The value of the  $P_{\text{in}}$  for each input port(s) and the control port is 1 W:

$$\text{ON/OFF contrast or extinction ratio (dB)} = 10 \log \left( \frac{P_{\text{out}}|\text{ON}}{P_{\text{out}}|\text{OFF}} \right), \quad (8)$$

where  $P_{\text{out}}|\text{ON}$  is the output optical power of the output port in case of ON state (logic 1).  $P_{\text{out}}|\text{OFF}$  is an output optical power of the output port in case of OFF state (logic 0).

When one port from the input port(s) or control port is in ON state, the transmission and output optical power have the same value. In this case, Eq. (8) will become Eq. (9):

$$\text{ON/OFF contrast or extinction ratio (dB)} = 10 \log \left( \frac{P_{\text{out}}|\text{ON}}{P_{\text{out}}|\text{OFF}} \right) = 10 \log \left( \frac{T_{\text{ON}}}{T_{\text{OFF}}} \right), \quad (9)$$

where  $T_{\text{ON}}$  is the transmission of optical power from the input port(s), and control port to the output port in case of ON state (logic 1); in other words,  $T_{\text{ON}}$  must be  $>0.25$  for all cases of the proposed plasmonic logic gates in the ON state, and  $T_{\text{OFF}}$  is the transmission of optical power from the input port(s), and control port to the output port in case of OFF state (logic 0); in other words,  $T_{\text{OFF}}$  must be  $<0.25$  in all cases of the proposed plasmonic logic gates in the OFF state.

Depending on the shape, size, and parameters of the proposed structure, materials, and refractive index of the chosen materials, the port position, the polarization of incident field and its phase, and the transmission of the optical power is minimized or maximized.

The interaction between stripes and nanorings causes new localized surface plasmon resonances, which are the results of the coupling between the nanorings resonator and the stripes (IMI). Furthermore, since plasmon waves couple strongly only in the near-field regime at very short distances, the coupling distance ( $d$ ) must be decreased to enable this mechanism to sustain and obtain the highest improvement of the field. Therefore, if the coupling distances increase, the field and the transmission spectrum decrease. According to the obtained results, the optimum coupling distance between the nanorings resonator and the stripes for the proposed structure has been chosen to be 7.5 nm.

On the other hand, the gate function for all proposed plasmonic logic gates is realized by the principle of constructive and destructive interferences between the input signal(s) and the control signal. Thus, the determination of these ports will decide the function of the plasmonic logic gate. The manipulation of the input port(s), control port, and the output port can achieve the required plasmonic logic gate. As we have already explained the reasons, surface plasmons are excited at the wavelength of 1550 nm for the seven proposed plasmonic logic gates.

The principle of the constructive and destructive interferences between the input light signal(s) and the control light signal depends on the phase of the incident light wave and the position of the input port(s) and control port when the other parameters (shape, size, dimensions of the structure, and materials used) remain unchanged.

The constructive interference occurs when the phase of incident wave of the ports (including the control port) as well as the direction of the propagation (depends on position of the ports) are the same, whereas the destructive interference happens when either the phase or the direction of the propagation of the incident wave of the ports are different.

As a result, the phase difference leads to destructive interference between the waves<sup>47</sup> according to Eq. (10):<sup>48</sup>

$$m = (4n_{\text{eff}}d \cos \theta)/\lambda, \quad (10)$$

where  $m$  is the interference order as an integer larger than 0,  $n_{\text{eff}}$  is an effective refractive index of the silver material,  $d$  is the thickness of the metal material,  $\theta$  is the phase of the incident wave, and  $\lambda$  is the incident wavelength.

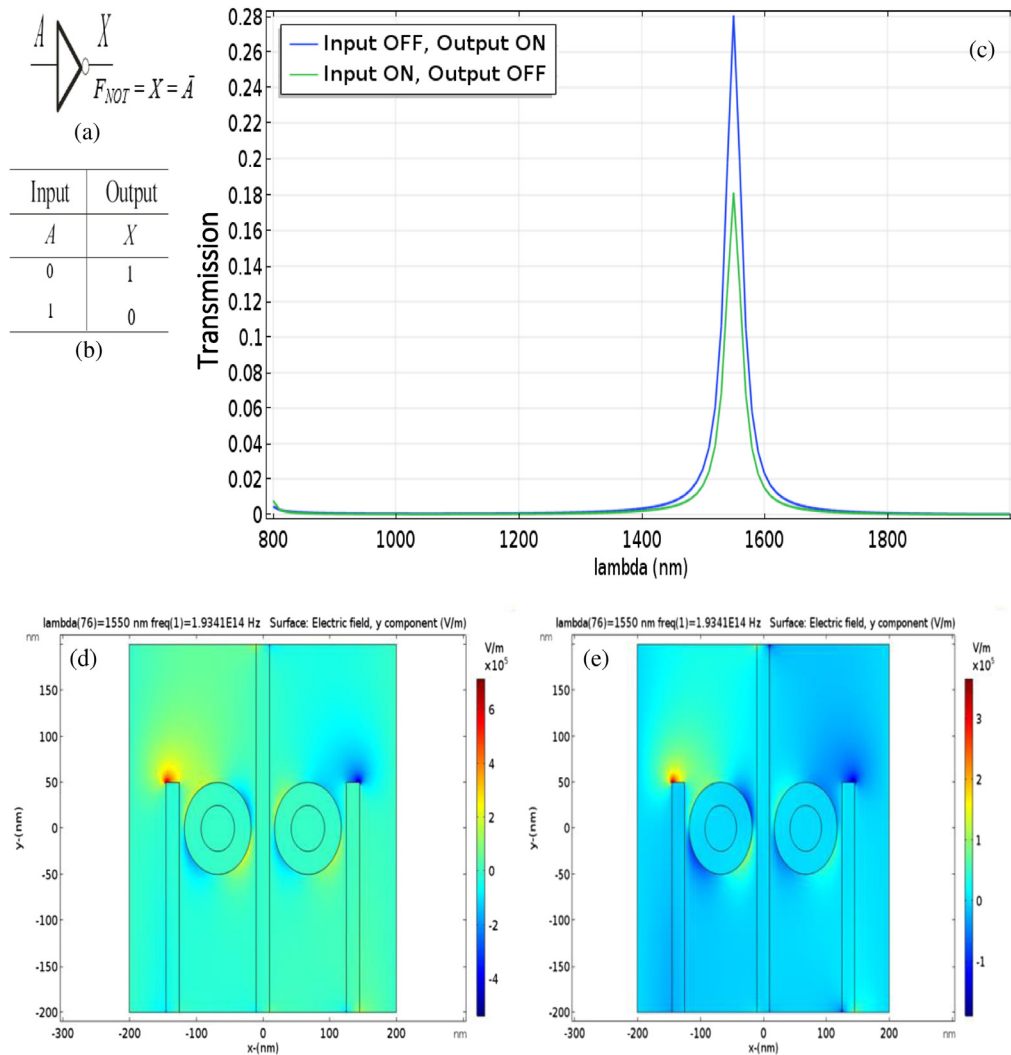
When  $\theta = 0$  deg, the sign of Eq. (10) is positive; this means the direction of the mode is the same direction of the propagation of the wave. Thus, constructive interference occurs with the other modes that have the same phase. As a result, the transmission will be increased.

When  $\theta = 90$  deg, Eq. (10) will be equal to zero, and neither constructive nor destructive interference will occur for this mode and the transmission is either increasing or decreasing depending on the other phases of input(s) and control light waves as well as the other parameters.

When  $\theta = 180$  deg, the sign of Eq. (10) is negative; this means the direction of the mode is in reverse direction of the propagation of the light wave. Thus, the destructive interference occurs with the other modes that have a different phase. As a result, the transmission will be decreased.

### 3 Proposed All-Optical Logic Gates

In all seven proposed plasmonic logic gates, the structure is illuminated by a plane wave with a wavelength ranging from 800 to 2000 nm. This illumination is launched to the input port(s) (ON state) and to the control port. To use the proposed structure (Fig. 1) as a structure to the all seven proposed plasmonic logic gates, the input port(s), the control port, and the output port must be determined to give the function of these proposed plasmonic logic gates. The process of



**Fig. 2** (a) and (b) The conventional symbol of a NOT logic gate and its truth table, respectively. (c) The transmission spectrum of the proposed plasmonic NOT logic gate at different states, according to its truth table. (d) and (e) The electric field distribution ( $y$ -component) of logic 1 and logic 0 outputs, respectively.



choosing these ports for the proposed plasmonic logic gates is done by trial-and-error method to give a better transmission performance and high contrast ratio.

### 3.1 Plasmonic NOT Logic Gate

A NOT gate, or inverter, is used to implement the complement concept in switching algebra. Thus, the logic value of the output of a NOT gate is simply the complement of the logic value of its input, according to Figs. 2(a) and 2(b).

To perform a NOT gate in our structure, we choose port 3 as an input port, port 4 as the output port, and port 1 as the control port, whereas port 2 is left as unused (see Fig. 1).

The function of this gate can be realized by the destructive interference between the input signal and the control signal. When the state of the input port is OFF and when the launching light at the wavelength of 1550 nm to the control port with a phase being equal to 180 deg, the state of the output port is ON according to the value of transmission that is 0.2807 (above transmission threshold = 0.25). When the launching light at the wavelength of 1550 nm to the input port and the control port (the state of the input port is ON) with the phase difference between them being 180 deg, then the destructive phenomenon will occur and the state of the output port is OFF according to the value of transmission that is 0.1811 (below transmission threshold = 0.25). The transmission spectrum of the proposed plasmonic NOT logic gate is shown in Fig. 2(c). Figures 2(d) and 2(e) show the electric field distribution (y-component) of logic 1 and logic 0 outputs, respectively. The operation of the proposed plasmonic NOT logic gate is summarized in Tables 2 and 3.

In plasmonic NOT logic gate, the contrast ratio is a negative value and low because the output optical power in OFF state is larger than the output optical power in ON state and the variance between the values of these powers is small, respectively. As a result, the transmission in the ON state is slightly higher than the threshold value and the transmission in the OFF state is slightly lower than the threshold value, which made the contrast ratio low.

### 3.2 Plasmonic OR Logic Gate

The output of the OR gate is logic 1 if at least one of the inputs is logic 1 and if all inputs are logic 0, the output is logic 0, according to Figs. 3(a) and 3(b). The OR operator is shown with a plus sign (+) between the variables.

To perform an OR gate in our structure, we choose port 1 as input port 1, port 2 as input port 2, port 4 as output port, and port 3 as control port.

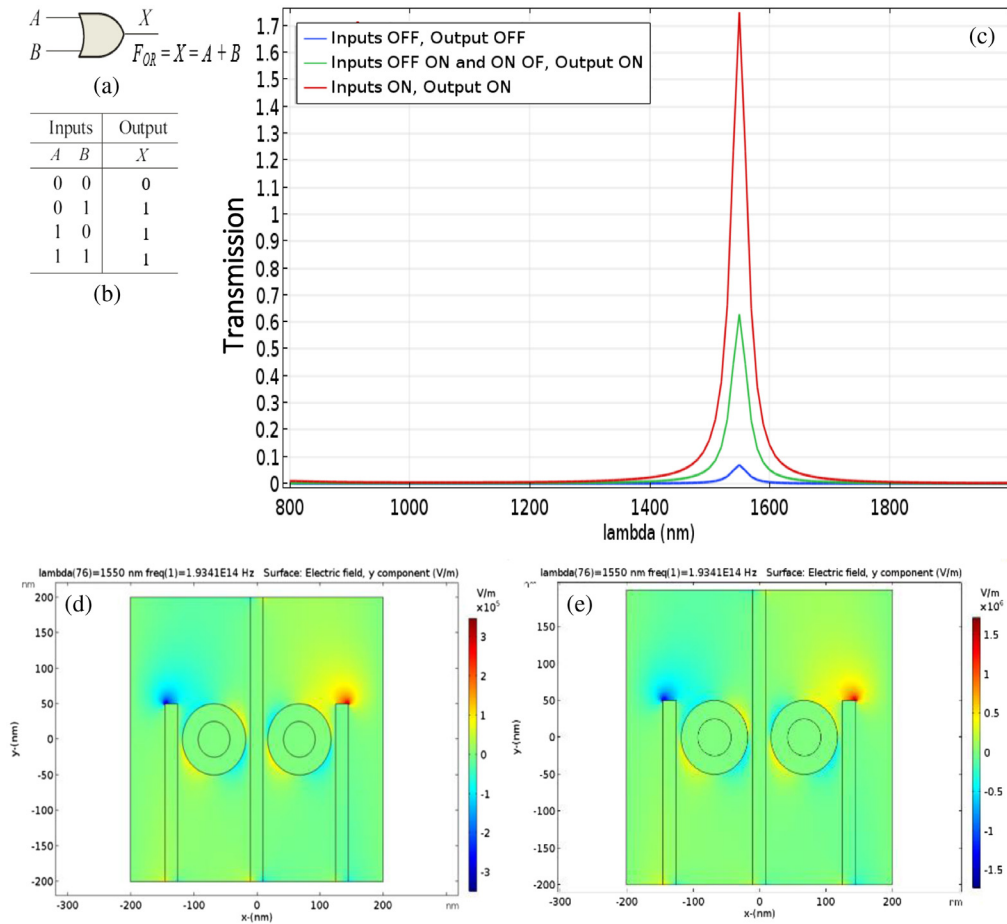
In the same manner of the proposed plasmonic NOT logic gate, the function of the proposed OR logic can be realized. Nevertheless, in this gate, it did not need to change the phase

**Table 2** Operation of the transmission for the proposed plasmonic NOT logic gate.

| Input state | Input port | Phase (deg) | Control port | Phase (deg) | $T$    | $T_{\text{thresh.}}$ | Output state | Output port |
|-------------|------------|-------------|--------------|-------------|--------|----------------------|--------------|-------------|
| Logic 0     | OFF        | 0           | ON           | 180         | 0.2807 | 0.25                 | Logic 1      | ON          |
| Logic 1     | ON         | 0           | ON           | 180         | 0.1811 | 0.25                 | Logic 0      | OFF         |

**Table 3** Calculation of the contrast ratio for the proposed plasmonic NOT logic gate.

| Input optical power/ port 1 (W) | Input optical power/ port 3 (W) | Total input optical power (W) | Output optical power (W) | Output state | Contrast ratio (dB) |
|---------------------------------|---------------------------------|-------------------------------|--------------------------|--------------|---------------------|
| 1                               | 0                               | 1                             | 0.2807                   | ON           | -1.1                |
| 1                               | 1                               | 2                             | 0.3622                   | OFF          |                     |



**Fig. 3** (a) and (b) The conventional symbol of an OR logic gate and its truth table, respectively. (c) The transmission spectrum of the proposed plasmonic OR logic gate at different states, according to its truth table. (d) and (e) The electric field distribution (y-component) when input ports are OFF and when input ports are ON, respectively.

shift between the input signal(s) and the control signal in order to get the maximum transmission in three cases. In this gate, the transmission exceeds 100% (1.75) when the two input ports and the control port are both in ON state. The enhancement and amplification of the transmission result from the constructive phenomenon between the input signals (1 and 2) and the control signal because the three signals have the same phase (0 deg). The transmission spectrum of the proposed plasmonic OR logic gate is shown in Fig. 3(c). Figures 3(d) and 3(e) show the electric field distribution (y-component) when input ports are OFF and when input ports are ON, respectively. The operation of the proposed plasmonic OR logic gate is summarized in Tables 4 and 5.

In Table 5, we note that the contrast ratio is high because the output optical power in ON states is large in comparison with the output optical power in OFF state (variance between  $P_{out}|ON$  and  $P_{out}|OFF$  is large, especially when the two input ports are in ON state). The best contrast ratio of this gate is when the two input ports are in ON state. As a result, the transmission in ON state is high in second and third states and exceeds 100% in forth state.

### 3.3 Plasmonic AND Logic Gate

The AND gate produces a logic 1 when all inputs are logic 1, otherwise, the output is logic 0, according to Figs. 4(a) and 4(b). The AND operator is usually shown with a dot between the variables, but it may be implied (no dot).



**Table 4** Operation of the transmission for the proposed plasmonic OR logic gate.

| Input state 1 | Input state 2 | Input port 1 | Phase (deg) | Input port 2 | Phase (deg) | Control port | Phase (deg) | $T$  | $T_{\text{thresh}}$ | Output state | Output port |
|---------------|---------------|--------------|-------------|--------------|-------------|--------------|-------------|------|---------------------|--------------|-------------|
| Logic 0       | Logic 0       | OFF          | 0           | OFF          | 0           | ON           | 0           | 0.07 | 0.25                | Logic 0      | OFF         |
| Logic 0       | Logic 1       | OFF          | 0           | ON           | 0           | ON           | 0           | 0.63 | 0.25                | Logic 1      | ON          |
| Logic 1       | Logic 0       | ON           | 0           | OFF          | 0           | ON           | 0           | 0.63 | 0.25                | Logic 1      | ON          |
| Logic 1       | Logic 1       | ON           | 0           | ON           | 0           | ON           | 0           | 1.75 | 0.25                | Logic 1      | ON          |

**Table 5** Calculation of the contrast ratio for the proposed plasmonic OR logic gate.

| Input optical power/ port 1 (W) | Input optical power/ port 2 (W) | Input optical power/ port 3 (W) | Total input optical power (W) | Output optical power (W) | Output state | Contrast ratio |
|---------------------------------|---------------------------------|---------------------------------|-------------------------------|--------------------------|--------------|----------------|
| 0                               | 0                               | 1                               | 1                             | 0.07                     | OFF          |                |
| 0                               | 1                               | 1                               | 2                             | 1.26                     | ON           | 12.55 dB       |
| 1                               | 0                               | 1                               | 2                             | 1.26                     | ON           | 18.75 dB       |
| 1                               | 1                               | 1                               | 3                             | 5.25                     | ON           |                |

In the AND gate structure, we choose input port 1 as port 1, input port 2 as port 2, output port as port 3, and control port as port 4.

The function of this gate can be realized by the constructive and destructive interferences between the input signal (s) and the control signal. When input ports are in OFF-ON and ON-OFF states (control port is in ON state always), the destructive interference occurs between the input signal and the control signal due to the phase difference (phase of the input signal = 180 deg and phase of control signal = 0 deg), which leads to the reduction in the transmission by 6%. On the other hand, when both input ports are in ON state, the constructive interference occurs between the input signals. As a result, the state of the output port is ON according to the value of the transmission that is 0.72 (above transmission threshold = 0.25). In this case, the transmission does not exceed 100% (72%), although the phase of input signals and the control signal is the same (phase = 0 deg), because the control port, namely port 4, has an opposed propagation direction in comparison with the input ports, which causes a destructive interference with the two input signals. The transmission spectrum of the proposed plasmonic AND logic gate is shown in Fig. 4(c). Figures 4(d) and 4(e) show the electric field distribution (y-component) when input ports are OFF-ON and when input ports are ON, respectively. The operation of the proposed plasmonic AND logic gate is summarized in Tables 6 and 7.

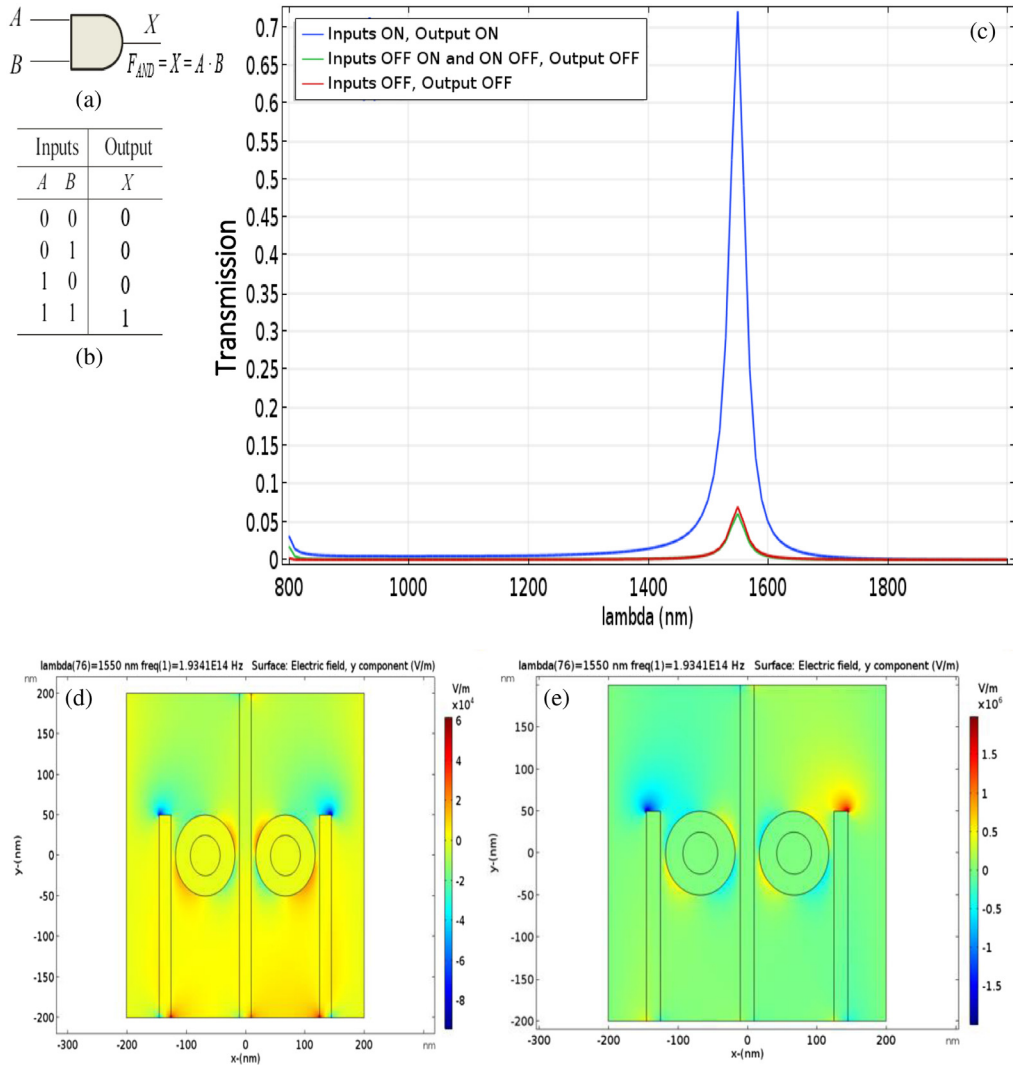
In Table 7, we note that the contrast ratio is high because the output optical power in ON states is large when compared with the output optical power in OFF states (variance between  $P_{\text{out}}|\text{ON}$  and  $P_{\text{out}}|\text{OFF}$  is large, especially when the two input ports are in OFF state). The best contrast ratio of this gate is when the two input ports are in OFF state. As a result, the transmission in ON state is high.

### 3.4 Plasmonic NOR Logic Gate

The NOR gate produces a logic 1 when all inputs are logic 0; otherwise, the output is logic 0, according to Figs. 5(a) and 5(b). The NOR operator is usually shown with a plus sign (+) between the variables and a complement sign covering them.

In the NOR gate structure, we choose input port 1 as port 2, input port 2 as port 3, output port as port 4, and control port as port 1.

The function of this gate can be achieved by destructive interference between the input signal (s) and the control signal. The first state (OFF–OFF) can be achieved in the same way as the first



**Fig. 4** (a) and (b) The conventional symbol of an AND logic gate and its truth table, respectively. (c) The transmission spectrum of the proposed plasmonic AND logic gate at different states, according to its truth table. (d) and (e) The electric field distribution (y-component) when input ports are OFF–ON and when input ports are ON, respectively.

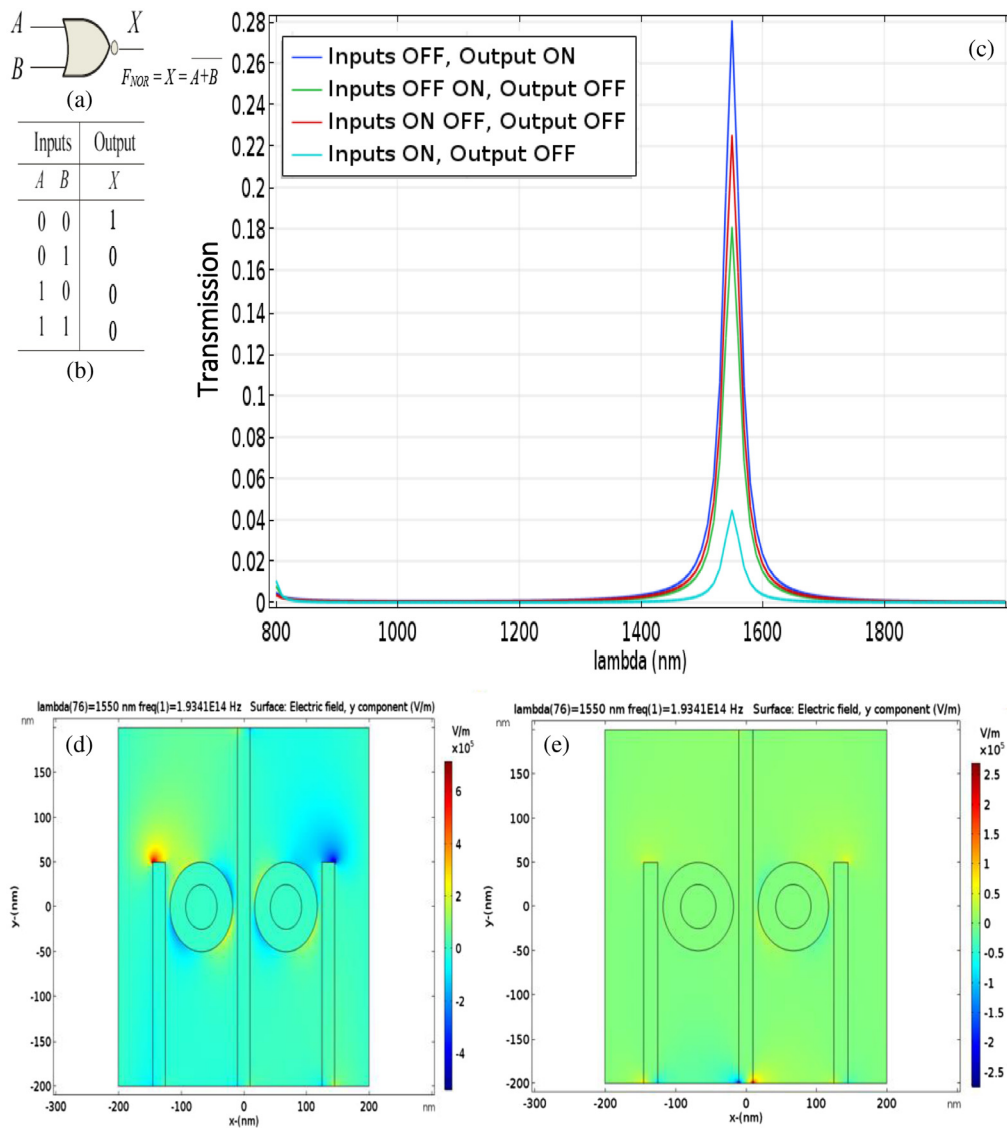
**Table 6** Operation of the transmission for the proposed plasmonic AND logic gate.

| Input state 1 | Input state 2 | Input port 1 | Phase (deg) | Input port 2 | Phase (deg) | Control port | Phase (deg) | T    | T <sub>thresh</sub> | Output state | Output port |
|---------------|---------------|--------------|-------------|--------------|-------------|--------------|-------------|------|---------------------|--------------|-------------|
| Logic 0       | Logic 0       | OFF          | 0           | OFF          | 0           | ON           | 0           | 0.07 | 0.25                | Logic 0      | OFF         |
| Logic 0       | Logic 1       | OFF          | 0           | ON           | 180         | ON           | 0           | 0.06 | 0.25                | Logic 0      | OFF         |
| Logic 1       | Logic 0       | ON           | 180         | OFF          | 0           | ON           | 0           | 0.06 | 0.25                | Logic 0      | OFF         |
| Logic 1       | Logic 1       | ON           | 0           | ON           | 0           | ON           | 0           | 0.72 | 0.25                | Logic 1      | ON          |

state of the proposed plasmonic NOT logic gate. In the other three states of the input ports (OFF–ON, ON–OFF, and ON–ON states), the output state is OFF due to the value of transmission is below the transmission threshold. In these three states, the destructive interference occurs due to the phase difference between the input signal(s) and the control signal. The transmission

**Table 7** Calculation of the contrast ratio for the proposed plasmonic AND logic gate.

| Input optical power/ port 1 (W) | Input optical power/ port 2 (W) | Input optical power/ port 4 (W) | Total input optical power (W) | Output optical power (W) | Output state | Contrast ratio (dB) |
|---------------------------------|---------------------------------|---------------------------------|-------------------------------|--------------------------|--------------|---------------------|
| 0                               | 0                               | 1                               | 1                             | 0.07                     | OFF          |                     |
| 0                               | 1                               | 1                               | 2                             | 0.12                     | OFF          | 14.89               |
| 1                               | 0                               | 1                               | 2                             | 0.12                     | OFF          | 12.55               |
| 1                               | 1                               | 1                               | 3                             | 2.16                     | ON           |                     |



**Fig. 5** (a) and (b) The conventional symbol of a NOR logic gate and its truth table, respectively. (c) The transmission spectrum of the proposed plasmonic NOR logic gate at different states, according to its truth table. (d) and (e) The electric field distribution (y-component) when input ports are OFF and when input ports are ON, respectively.

**Table 8** Operation of the transmission for the proposed plasmonic NOR logic gate.

| Input state 1 | Input state 2 | Input port 1 | Phase (deg) | Input port 2 | Phase (deg) | Control port | Phase (deg) | $T$    | $T_{\text{thresh}}$ | Output state | Output port |
|---------------|---------------|--------------|-------------|--------------|-------------|--------------|-------------|--------|---------------------|--------------|-------------|
| Logic 0       | Logic 0       | OFF          | 0           | OFF          | 0           | ON           | 180         | 0.2807 | 0.25                | Logic 1      | ON          |
| Logic 0       | Logic 1       | OFF          | 0           | ON           | 0           | ON           | 180         | 0.1811 | 0.25                | Logic 0      | OFF         |
| Logic 1       | Logic 0       | ON           | 0           | OFF          | 0           | ON           | 180         | 0.2254 | 0.25                | Logic 0      | OFF         |
| Logic 1       | Logic 1       | ON           | 0           | ON           | 90          | ON           | 180         | 0.045  | 0.25                | Logic 0      | OFF         |

**Table 9** Calculation of the contrast ratio for the proposed plasmonic NOR logic gate.

| Input optical power/ port 2 (W) | Input optical power/ port 3 (W) | Input optical power/ port 1 (W) | Total input optical power (W) | Output optical power (W) | Output state | Contrast ratio |
|---------------------------------|---------------------------------|---------------------------------|-------------------------------|--------------------------|--------------|----------------|
| 0                               | 0                               | 1                               | 1                             | 0.2807                   | ON           |                |
| 0                               | 1                               | 1                               | 2                             | 0.3622                   | OFF          | -1.1 dB        |
| 1                               | 0                               | 1                               | 2                             | 0.4508                   | OFF          | -2 dB          |
| 1                               | 1                               | 1                               | 3                             | 0.135                    | OFF          | 3.18 dB        |

spectrum of the proposed plasmonic NOR logic gate is shown in Fig. 5(c). Figures 5(d) and 5(e) show the electric field distribution ( $y$ -component) when the input ports are OFF and when the input ports are ON, respectively. The operation of the proposed plasmonic NOR logic gate is summarized in Tables 8 and 9.

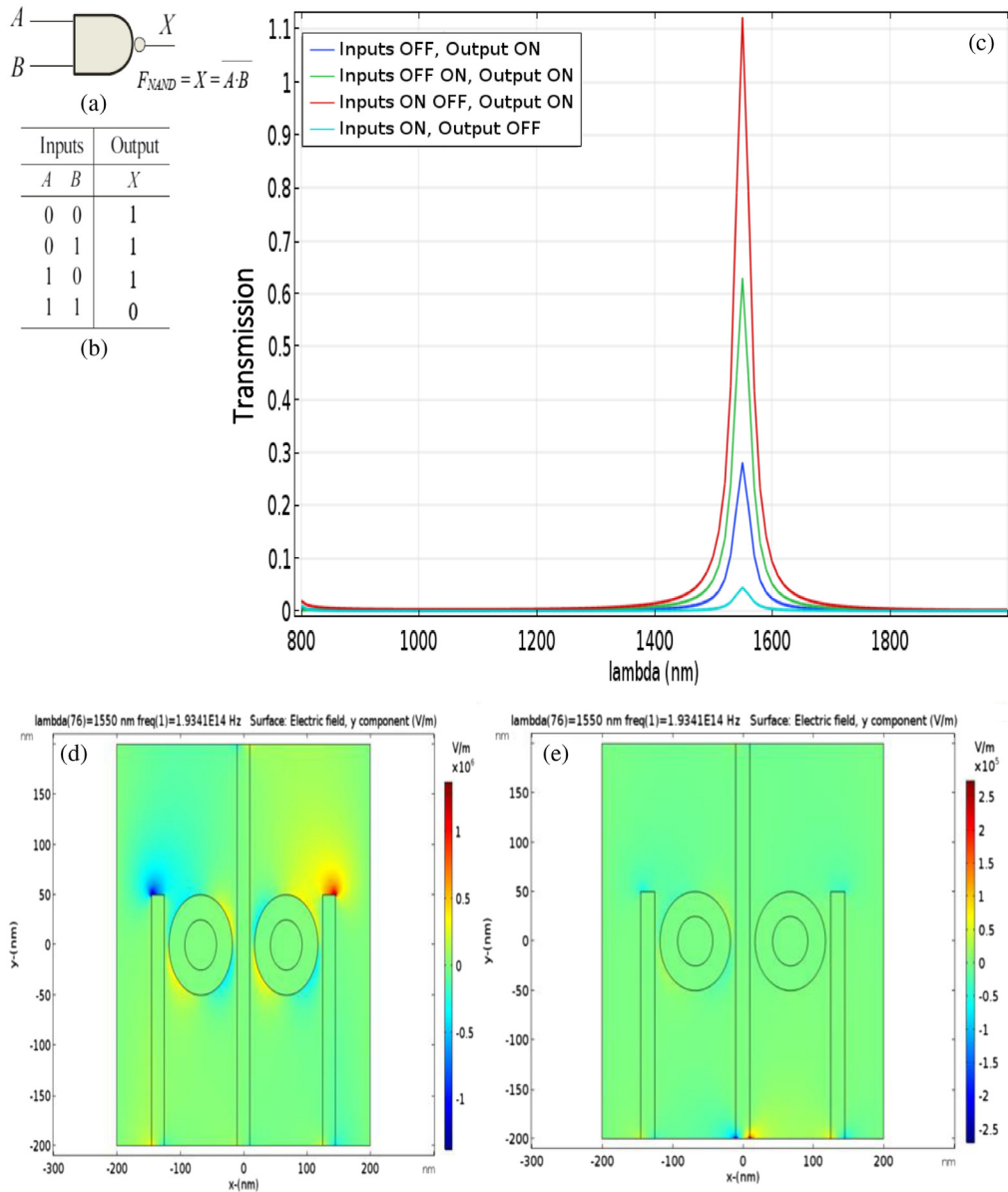
In Table 9, we note that the contrast ratio is a negative value (first and second values) and low because the output optical power in OFF states (first and second states) is larger than the output optical power in ON state and the variance between the values of these powers is small, respectively. The best contrast ratio of this gate is when the two input ports are in ON state. As a result, the transmission in ON state is slightly higher than the threshold value and the transmission in the OFF state is slightly lower than the threshold value (second and third states).

### 3.5 Plasmonic NAND Logic Gate

The NAND gate produces a logic 0 when all inputs are logic 1; otherwise, the output is logic 1, according to Figs. 6(a) and 6(b). The NAND operator is shown with a dot between the variables and a complement sign covering them.

In the NAND gate structure, we choose input port 1 as port 2, input port 2 as port 3, the output port as port 4, and control port as port 1 (similar to the NOR gate).

The function of this gate can be achieved by the enhancement and suppression interferences between the input signal(s) and the control signal. When the state of the input ports is OFF and when the launching light at the wavelength of 1550 nm to the control port with phase being always equal to 0 deg, the state of the output port is ON according to the value of transmission that is 0.2807 (above transmission threshold = 0.25). In this state, neither constructive nor destructive interference occurs because only one port is in ON state (control port). As a result, the transmission is slightly above the threshold. In the second state (OFF–ON state), the transmission is 0.63 (above transmission threshold = 0.25), which is regarded as a logic 1. In the second state, the transmission does not exceed 100%, although the phase of these ports is equal. This is because the length of stripes of the control port and the input port 2 is unequal. In the third state (ON–OFF state), the amplification to the transmission occurs (transmission = 1.123), which



**Fig. 6** (a) and (b) The conventional symbol of a NAND logic gate and its truth table, respectively. (c) The transmission spectrum of the proposed plasmonic NAND logic gate at different states, according to its truth table. (d) and (e) The electric field distribution ( $y$ -component) when input ports are ON–OFF and when input ports are ON, respectively.

is regarded as a logic 1 also. In this case, the constructive interference occurs between the input signal and a control signal, which leads to the transmission exceeding 100%. In the fourth case (ON–ON), the transmission is 0.045, which is regarded as a logic 0. In this case, destructive interference occurs between input signals and control signal due to the difference in phase. The transmission spectrum of the proposed plasmonic NAND logic gate is shown in Fig. 6(c). Figures 6(d) and 6(e) show the electric field distribution ( $y$ -component) when input ports are ON–OFF and when input ports are ON, respectively. The operation of the proposed plasmonic NAND logic gate is summarized in Tables 10 and 11.

In Table 11, we note that the contrast ratio is high (second and third states) and low in first ON state. The best contrast ratio of this gate is when the two input ports are in ON–OFF state. As a result, the transmission in ON state is high in the second state and exceeds 100% in the third state, but slightly higher than the threshold value in the first state that makes the contrast ratio is low.

**Table 10** Operation of the transmission for the proposed plasmonic NAND logic gate.

| Input state 1 | Input state 2 | Input port 1 | Phase (deg) | Input port 2 | Phase (deg) | Control port | Phase (deg) | $T$    | $T_{\text{thresh}}$ | Output state | Output port |
|---------------|---------------|--------------|-------------|--------------|-------------|--------------|-------------|--------|---------------------|--------------|-------------|
| Logic 0       | Logic 0       | OFF          | 0           | OFF          | 0           | ON           | 0           | 0.2807 | 0.25                | Logic 1      | ON          |
| Logic 0       | Logic 1       | OFF          | 0           | ON           | 0           | ON           | 0           | 0.63   | 0.25                | Logic 1      | ON          |
| Logic 1       | Logic 0       | ON           | 0           | OFF          | 0           | ON           | 0           | 1.123  | 0.25                | Logic 1      | ON          |
| Logic 1       | Logic 1       | ON           | 180         | ON           | 90          | ON           | 0           | 0.045  | 0.25                | Logic 0      | OFF         |

**Table 11** Calculation of the contrast ratio for the proposed plasmonic NAND logic gate.

| Input optical power/ port 2 (W) | Input optical power/ port 3 (W) | Input optical power/ port 1 (W) | Total input optical power (W) | Output optical power (W) | Output state | Contrast ratio (dB) |
|---------------------------------|---------------------------------|---------------------------------|-------------------------------|--------------------------|--------------|---------------------|
| 0                               | 0                               | 1                               | 1                             | 0.2807                   | ON           |                     |
| 0                               | 1                               | 1                               | 2                             | 1.26                     | ON           | 3.12<br>9.7         |
| 1                               | 0                               | 1                               | 2                             | 2.246                    | ON           | 12.2                |
| 1                               | 1                               | 1                               | 3                             | 0.135                    | OFF          |                     |

### 3.6 Plasmonic XOR Logic Gate

The XOR gate produces a logic 1 output only when both inputs are at opposite logic levels; otherwise, the output is logic 0, according to Figs. 7(a) and 7(b). The XOR operator is usually shown with a circled plus sign ( $\oplus$ ) between the variables  $A$  and  $B$ .

In XOR gate structure, we choose input port 1 as port 1, input port 2 as port 2, the output port as port 4, and control port as port 3 (similar to the OR gate).

At this plasmonic logic gate (OFF–ON and ON–OFF states), the constructive interference between the input signal and the control signal is not large. However, the transmission = 0.63, which is regarded as logic 1. In the fourth state (ON–ON), destructive interference occurred between the input signals and the control signal due to the difference in the signal phase. Thus, the transmission diminished to 0.087, which is regarded to logic 0. The transmission spectrum of the proposed plasmonic XOR logic gate is shown in Fig. 7(c). Figures 7(d) and 7(e) show the electric field distribution ( $y$ -component) when input ports are ON–OFF and when input ports are ON, respectively. The operation of the proposed plasmonic XOR logic gate is summarized in Tables 12 and 13.

In Table 13, we note that the contrast ratio is high (first OFF state) and moderate (second OFF state) because the output optical power in ON states is large in comparison with the output optical power in OFF states (variance between  $P_{\text{out}}|\text{ON}$  and  $P_{\text{out}}|\text{OFF}$  is large, especially when the two input ports are in OFF state).

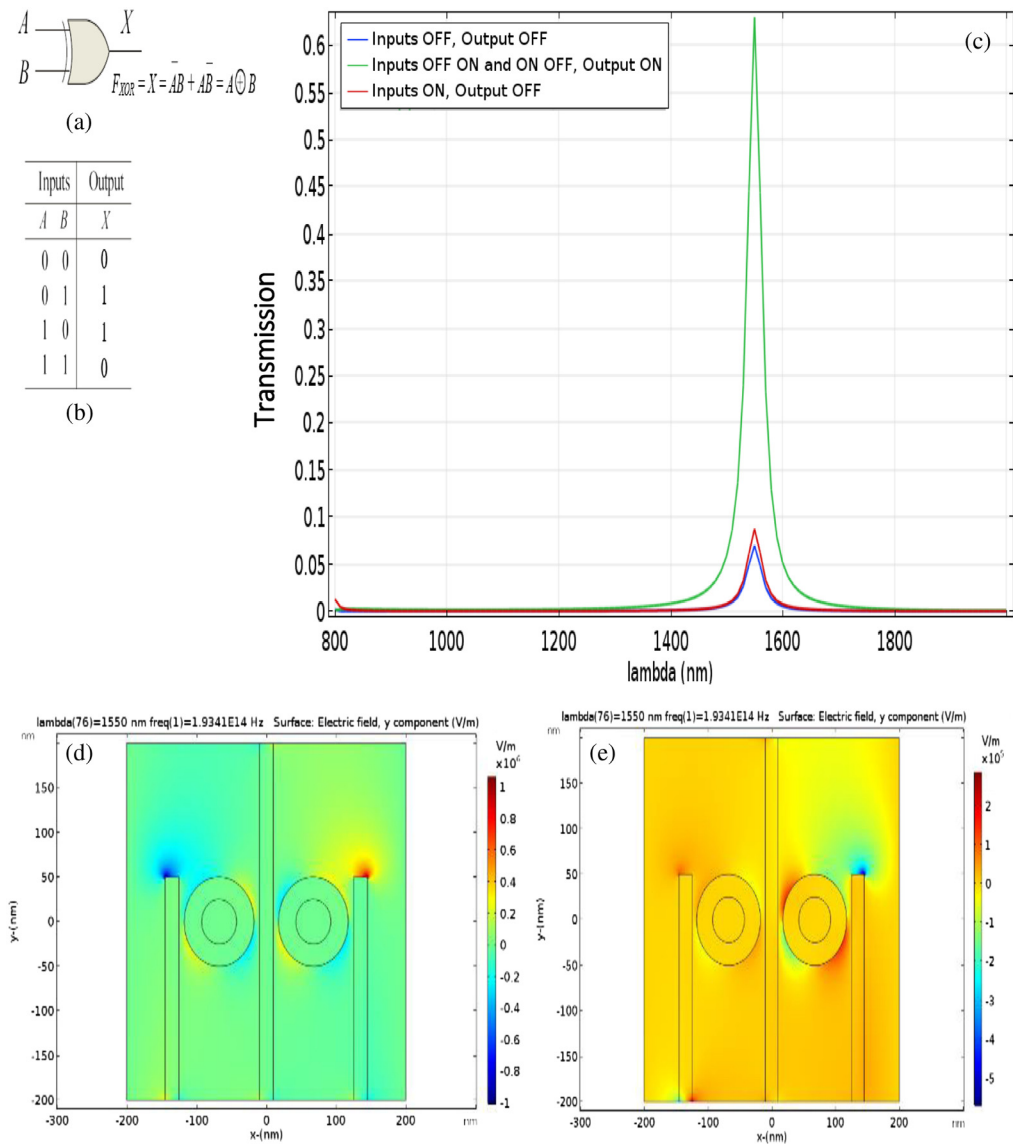
### 3.7 Plasmonic XNOR Logic Gate

The XNOR gate produces a logic 1 output only when both inputs are in the same logic levels; otherwise, the output is logic 0, according to Figs. 8(a) and 8(b). The XNOR operator is usually shown with a circled plus sign ( $\oplus$ ) between the variables and a complement sign covering them.

In XNOR gate structure, the input ports, control port, and output port are the same ports of the NOR gate and NAND gate structures.

The function of this gate can be achieved by the constructive and destructive interferences between the input signal ( $s$ ) and the control signal. The first state (OFF–OFF) can be achieved in the same way as we obtained in the first state of the proposed plasmonic NOT logic gate. In the second and the third states (OFF–ON and ON–OFF), the destructive interference happens





**Fig. 7** (a) and (b) The conventional symbol of a XOR logic gate and its truth table, respectively. (c) The transmission spectrum of the proposed plasmonic XOR logic gate at different states, according to its truth table. (d) and (e) The electric field distribution (y-component) when input ports are ON–OFF and when input ports are ON, respectively.

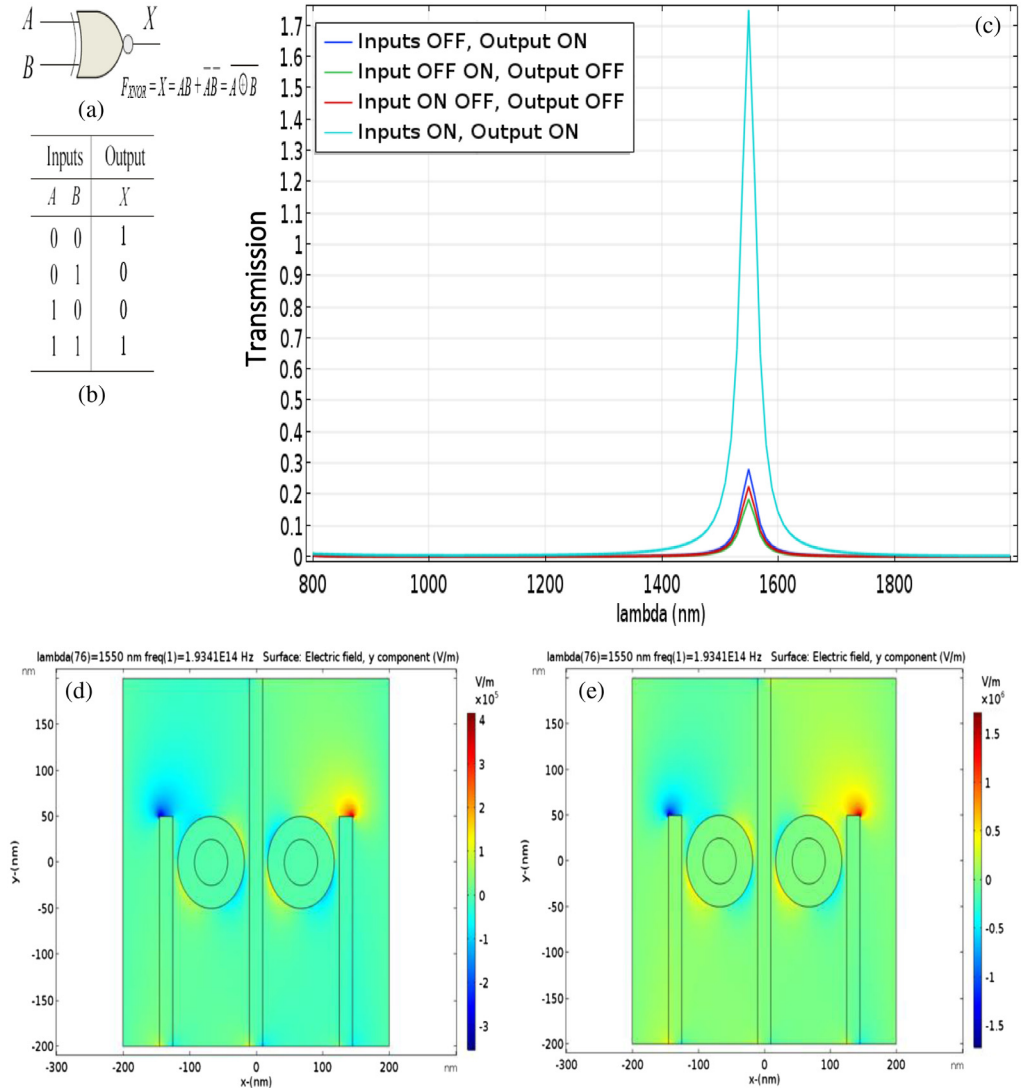
**Table 12** Operation of the transmission for the proposed plasmonic XOR logic gate.

| Input state 1 | Input state 2 | Input port 1 | Phase (deg) | Input port 2 | Phase (deg) | Control port | Phase (deg) | T     | T <sub>thresh</sub> | Output state | Output port |
|---------------|---------------|--------------|-------------|--------------|-------------|--------------|-------------|-------|---------------------|--------------|-------------|
| Logic 0       | Logic 0       | OFF          | 0           | OFF          | 0           | ON           | 0           | 0.07  | 0.25                | Logic 0      | OFF         |
| Logic 0       | Logic 1       | OFF          | 0           | ON           | 0           | ON           | 0           | 0.63  | 0.25                | Logic 1      | ON          |
| Logic 1       | Logic 0       | ON           | 0           | OFF          | 0           | ON           | 0           | 0.63  | 0.25                | Logic 1      | ON          |
| Logic 1       | Logic 1       | ON           | 180         | ON           | 90          | ON           | 0           | 0.087 | 0.25                | Logic 0      | OFF         |

between the input signal and control signal due to the difference in phase. Thus, the transmission is less than the threshold and is regarded as logic 0. In the fourth state (ON–ON), the large constructive interference happens between the input signals and the control signal due to the

**Table 13** Calculation of contrast ratio for the proposed plasmonic XOR logic gate.

| Input optical power/ port 1 (W) | Input optical power/ port 2 (W) | Input optical power/ port 3 (W) | Total input optical power (W) | Output optical power (W) | Output state | Contrast ratio (dB) |
|---------------------------------|---------------------------------|---------------------------------|-------------------------------|--------------------------|--------------|---------------------|
| 0                               | 0                               | 1                               | 1                             | 0.07                     | OFF          |                     |
| 0                               | 1                               | 1                               | 2                             | 1.26                     | ON           | 12.55               |
| 1                               | 0                               | 1                               | 2                             | 1.26                     | ON           | 6.84                |
| 1                               | 1                               | 1                               | 3                             | 0.261                    | OFF          |                     |



**Fig. 8** (a) and (b) The conventional symbol of an XNOR logic gate and its truth table, respectively. (c) The transmission spectrum of the proposed plasmonic XNOR logic gate at different states according to its truth table. (d) and (e) The electric field distribution (y-component) when input ports are OFF–ON and when input ports are ON, respectively.

similar phase of these signals (phase = 0 deg). This results in amplifying the transmission to be above 100% (175%) and that is regarded as logic 1. The transmission spectrum of the proposed plasmonic XNOR logic gate is shown in Fig. 7(c). Figures 7(d) and 7(e) show the electric field distribution (y-component) when input ports are OFF–ON and when input ports are ON,

**Table 14** Operation of the transmission for the proposed plasmonic XNOR logic gate.

| Input state 1 | Input state 2 | Input port 1 | Phase (deg) | Input port 2 | Phase (deg) | Control port | Phase (deg) | $T$    | $T_{\text{thresh}}$ | Output state | Output port |
|---------------|---------------|--------------|-------------|--------------|-------------|--------------|-------------|--------|---------------------|--------------|-------------|
| Logic 0       | Logic 0       | OFF          | 0           | OFF          | 0           | ON           | 0           | 0.2807 | 0.25                | Logic 1      | ON          |
| Logic 0       | Logic 1       | OFF          | 0           | ON           | 180         | ON           | 0           | 0.185  | 0.25                | Logic 0      | OFF         |
| Logic 1       | Logic 0       | ON           | 180         | OFF          | 0           | ON           | 0           | 0.2254 | 0.25                | Logic 0      | OFF         |
| Logic 1       | Logic 1       | ON           | 0           | ON           | 0           | ON           | 0           | 1.75   | 0.25                | Logic 1      | ON          |

**Table 15** Calculation of the contrast ratio for the proposed plasmonic XNOR logic gate.

| Input optical power/ port 2 (W) | Input optical power/ port 3 (W) | Input optical power/ port 1 (W) | Total input optical power (W) | Output optical power (W) | Output state | Contrast ratio (dB) |
|---------------------------------|---------------------------------|---------------------------------|-------------------------------|--------------------------|--------------|---------------------|
| 0                               | 0                               | 1                               | 1                             | 0.2807                   | ON           |                     |
| 0                               | 1                               | 1                               | 2                             | 0.37                     | OFF          | -1.2<br>-2          |
| 1                               | 0                               | 1                               | 2                             | 0.4508                   | OFF          | 11.74<br>10.88      |
| 1                               | 1                               | 1                               | 3                             | 5.52                     | ON           |                     |

respectively. The operation of the proposed plasmonic XNOR logic gate is summarized in Tables 14 and 15.

In Table 15, we express four values for contrast ratio: the first and second values are negative and low, because  $P_{\text{out}}|\text{OFF}$  is larger than  $P_{\text{out}}|\text{ON}$  and the variance between them is small; and the third and fourth values are high because  $P_{\text{out}}|\text{ON}$  is larger than  $P_{\text{out}}|\text{OFF}$  and the variance between them is large. The best contrast ratio of this gate can be obtained when the two input ports are in OFF-ON and ON states. As a result, the transmission in ON state is high and exceeds 100% in the fourth state but slightly higher than the threshold value in the first state, which makes the contrast ratio low and negative.

#### 4 Comparison between the Proposed Work and the Previous Works

The proposed plasmonic logic gates are compared to the previous papers as depicted in Table 16.

#### 5 Conclusion

In this paper, seven plasmonic logic gates have been proposed and realized using 2-D FEM. These gates are NOT, OR, AND, NOR, NAND, XOR, and XNOR. The gates are constructed by the nanoring IMI plasmonic structure. By employing the coupling property between straight stripes and ring resonator waveguides, we can achieve a plasmonic logic gate. By changing the state of the input port (s), the position of the input port(s) and a control port, and the phase of incident light in these ports, we can make the transmission in the output port minimized or maximized according to the required plasmonic logic gate. To give a decision that the proposed plasmonic logic gate is investigating the truth table of one of the logic gates, we have established a threshold value of transmission to distinguish between logic 1 and logic 0 states. The proposed value of transmission threshold is 0.25% or 25%, and choosing this value achieves seven plasmonic logical gates in one structure. Finally, the proposed plasmonic logic gates are considered fundamental building blocks in photonic integrated circuits and all-optical signal-processing systems.

**Table 16** Comparison between our proposed plasmonic logic gates and previous papers.

| Criteria   | This paper   | Ref. 25   | Ref. 26  | Ref. 27   | Ref. 28  | Ref. 29  |
|--|--|---|--|---|--|--|
| Software program used  | FEM-2D   | FDTD-2-D  | FDTD-2-D   | FDTD-2-D  | FDTD-2-D   | FDTD-2-D   |
| Proposed structure   | Nanoring IMI plasmonic nanowaveguides                            | MIM-plasmonic waveguides with nanodisk resonator                  | Microfing MIM plasmonic waveguides                             | Square microfing MIM nonlinear plasmonic waveguides               | Plasmonic MIM nanowaveguides with slot cavity resonator          | Ring resonator MIM plasmonic waveguides                          |
| Number of proposed logic gates                               | 7 gates  | 4 gates   | 1 gate   | 3 gates   | 3 gates  | 2 gates  |
| Proposed logic gates   | NOT, OR, AND, NOR, NAND, XOR, and XNOR                           | NOT, NAND, XOR, and XNOR  | NOT  | NOT, AND, and NOR   | NOT, OR, and XOR   | AND and NOR  |
| Realization of proposed plasmonic logic gates                | All proposed plasmonic logic gates are realized in one structure | The proposed plasmonic logic gates are realized in two structures | The proposed plasmonic logic gate is realized in one structure | The proposed plasmonic logic gates are realized in two structures | The proposed plasmonic logic gates are realized in one structure | The proposed plasmonic logic gates are realized in one structure |
| Size   | 400 nm × 400 nm  | 1220 nm × 1120 nm   | 2.4 μm × 3 μm  | 750 nm × 900 nm and 1.5 μm × 1.8 μm                               | 760 nm × 600 nm  | More than 3 μm × 2 μm  |
| Operating wavelength(s)                                      | 1550 nm  | 525 nm  | 850 nm   | 1535 nm   | 1535 nm  | 944 nm and 999 nm  |
| Dielectric material used                                     | Teflon   | Air   | Air  | SiO <sub>2</sub>  | Air  | Air  |
| Nobel metal used   | Silver   | Silver  | Silver   | Silver  | Silver   | Silver   |
| Model of description the relative permittivity of the silver | Johnson and Christy data   | Drude model   | Drude model  | Drude model   | Drude model  | Drude model  |

**Table 16 (Continued).**

| Criteria                                     | This paper   | Ref. 25   | Ref. 26            | Ref. 27   | Ref. 28  | Ref. 29                                 |
|--|--|---|--------------------|---|--|---|
| Performance measured                         | Transmission and contrast ratio  | Transmission and contrast ratio                         | Transmission       | Transmission  | Transmission and contrast ratio                      | Transmission and contrast ratio         |
| Transmission threshold between ON/OFF states | 0.25% or 25%   | 0.1% or 10%   | 0.2% or 20%        | 0.35% or 35%  | 0.3% or 30%  | 0.5% or 50% or less                     |
| Maximum transmission %                       | 28.07% at NOT gate<br>175% at OR gate<br>72% at AND gate<br>28.07% at NOR gate<br>112.3% at NAND gate<br>63% at XOR gate<br>175% at XNOR gate<br>Exists in OR gate, NAND gate, and XNOR gate | 25% at NAND gate<br>42% at XOR gate<br>25% at XNOR gate | 65.35% at NOT gate | 70% at NOT gate<br>70% at NOR gate<br>90% at AND gate | 38% at NOT gate<br>80% at OR gate<br>40% at XOR gate | 84.06% at AND gate<br>80.07 at NOR gate |
| Amplifying of transmission                   |  | Does not exist  | Does not exist     | Does not exist  | Does not exist                                       | Does not exist                          |

## References

1. H. J. Lezec et al., “Beaming light from a subwavelength aperture,” *Science* **297**(5582), 820–822 (2002).
2. X. Mei, X. G. Huang, and T. Jin, “A sub-wavelength electro-optic switch based on plasmonic T-shaped waveguide,” *Plasmonics* **6**(4), 613–618 (2011).
3. X. Peng et al., “Research on transmission characteristics of aperture-coupled square-ring resonator based filter,” *Opt. Commun.* **294**, 368–371 (2013).
4. B. Wang and G. P. Wang, “Plasmon bragg reflectors and nanocavities on flat metallic surfaces,” *Appl. Phys. Lett.* **87**(1), 013107 (2005).
5. J. Chen et al., “Plasmonic Y-splitters of high wavelength resolution based on strongly coupled resonator effects,” *Plasmonics* **7**(3), 441–445 (2012).
6. Y. Guo et al., “Transmission characteristics of the aperture-coupled rectangular resonators based on metal-insulator-metal waveguides,” *Opt. Commun.* **300**, 277–281 (2013).
7. N. Nozhat and N. Granpayeh, “Switching power reduction in the ultracompact Kerr nonlinear plasmonic directional coupler,” *Opt. Commun.* **285**(6), 1555–1559 (2012).
8. Z. Lu and W. Zhao, “Nanoscale electro-optic modulators based on graphene-slot waveguides,” *J. Opt. Soc. Am. B* **29**(6), 1490–1496 (2012).
9. N. Nozhat and N. Granpayeh, “Analysis of the plasmonic power splitter and MUX/DEMUX suitable for photonic integrated circuits,” *Opt. Commun.* **284**(13), 3449–3455 (2011).
10. H. Li et al., “Enhanced optical forces in integrated hybrid plasmonic waveguides,” *Opt. Express* **21**(10), 11839–11851 (2013).
11. J. Tao, Q. J. Wang, and X. G. Huang, “All-optical plasmonic switches based on coupled nanodisk cavity structures containing nonlinear material,” *Plasmonics* **6**(4), 753–759 (2011).
12. N. Nozhat and N. Granpayeh, “All-optical nonlinear plasmonic ring resonator switches,” *J. Mod. Opt.* **61**(20), 1690–1695 (2014).
13. Y. Liu et al., “All-optical logic gates based on two-dimensional low-refractive-index nonlinear photonic crystal slabs,” *Opt. Express* **19**(3), 1945–1953 (2011).
14. D. Pan, H. Wei, and H. Xu, “Optical interferometric logic gates based on metal slot waveguide network realizing whole fundamental logic operations,” *Opt. Express* **21**(8), 9556–9562 (2013).
15. L. Wang et al., “Optical quasi logic gates based on polarization-dependent four-wave mixing in subwavelength metallic waveguides,” *Opt. Express* **21**(12), 14442–14451 (2013).
16. Y. Bian and Q. Gong, “Compact all-optical interferometric logic gates based on one-dimensional metal-insulator-metal structures,” *Opt. Commun.* **313**, 27–35 (2014).
17. K. J. A. Ooi et al., “Electro-optical graphene plasmonic logic gates,” *Opt. Lett.* **39**(6), 1629–1632 (2014).
18. I. S. Maksymov, “Optical switching and logic gates with hybrid plasmonic-photonic crystal nanobeam cavities,” *Phys. Lett. A* **375**(5), 918–921 (2011).
19. S. Kaur and R. S. Kaler, “Ultrahigh speed reconfigurable logic operations based on single semiconductor optical amplifier,” *J. Opt. Soc. Korea* **16**(1), 13–16 (2011).
20. G. Y. Oh, D. G. Kim, and Y. W. Choi, “Conference All-optical logic gate using waveguide-type SPR with Au/ZnO plasmon stack,” in *Proc. Opto Electron. and Commun.*, Japan, pp. 374–375 (2010).
21. Q. Xu and M. Lispon, “All-optical logic based on silicon micro-ring resonators,” *Opt. Express* **15**(3), 924–929 (2007).
22. T. K. Liang et al., “High speed logic gate using two photon absorption in silicon waveguides,” *Opt. Commun.* **265**(1), 171–174 (2006).
23. J. H. Kim et al., “All-optical AND gate using XPM wavelength converter,” *J. Opt. Soc. Korea* **5**(1), 25–28 (2001).
24. H. Wei et al., “Cascaded logic gates in nanophotonic plasmon networks,” *Nat. Commun.* **2**(1), 387 (2011).
25. A. Dolatabady and N. Granpayeh, “All optical logic gates based on two dimensional plasmonic waveguides with nanodisk resonators,” *J. Opt. Soc. Korea* **16**(4), 432–442 (2012).
26. Y.-D. Wu, Y.-T. Hsueh, and T.-T. Shih, “Novel all-optical logic gates based on microring metal-insulator-metal plasmonic waveguides,” in *PIERS Proc.*, pp. 169–172 (2013).



27. N. Nozhat and N. Granpayeh, “All-optical logic gates based on nonlinear plasmonic ring resonators,” *Appl. Opt.* **54**(26), 7944–7948 (2015).
28. A. Dolatabady and N. Granpayeh, “All-optical logic gates in plasmonic metal-insulator–metal nanowaveguide with slot cavity resonator,” *J. Nanophotonics* **11**(2), 026001 (2017).
29. Z. Liu et al., “Design of a multi-bits input optical logic device with high intensity contrast based on plasmonic waveguides structure,” *Opt. Commun.* **430**, 112–118 (2019).
30. R. Zia et al., “Geometries and materials for subwavelength surface plasmon modes,” *J. Opt. Soc. Am.* **21**(12), 2442–2446 (2004).
31. Z. Han and S. I. Bozhevolnyi, “Radiation guiding with surface plasmon polaritons,” *Rep. Prog. Phys.* **76**(1), 016402 (2013).
32. S. Kedia and J. Kedia, “Hybrid plasmonic waveguide—a review,” *Int. J. Sci. Res. Dev.* **5**(4), 1910–1913 (2017).
33. P. Berini, “Figures of merit for surface plasmon waveguides,” *Opt. Express* **14**(26), 1303–13042 (2006).
34. C. Zhong, “Plasmonic waveguides for sub-wavelength light confinement,” Doctoral Thesis, Trinity College Dublin, the University of Dublin (2018).
35. S. Ishii et al., “Plasmonic waveguides clad by hyperbolic metamaterials,” *Opt. Lett.* **39**(16), 4663–4666 (2014).
36. X. Sun et al., “Comparison of confinement and loss of plasmonic waveguides,” in *IEEE Photonics Conf.*, pp. 618–619 (2012).
37. K. Tong et al., “IMI long-range surface plasmon Bragg micro-cavity,” *Mod. Phys. Lett. B* **30**(30), 1650355 (2016).
38. J. Leuthold, “Plasmonic: communications light on a wire,” *Opt. Photonics News* **24**(5), 28–35 (2013).
39. B. Dastmalchi et al., “A new perspective on plasmonics: confinement and propagation length of surface plasmons for different materials and geometries,” *Adv. Opt. Mater.* **4**(1), 177–184 (2016).
40. Y. Chowdhury, “Plasmonic waveguides: design and comparative study,” MSc Thesis, Royal Institute of Technology (2011).
41. H. Hirori, M. Nagai, and K. Tanaka, “Destructive interference effect on surface plasmon resonance in terahertz attenuated total reflection,” *Opt. Express* **13**(26), 10801–10814 (2005).
42. P. B. Johnson and R. W. Christy, “Optical constants of the noble metals,” *Phys. Rev.* **6**(12), 4370–4379 (1972).
43. R. H. French et al., “Optical properties of materials for concentrator photovoltaic systems,” in *34th IEEE Photovoltaic Specialists Conf. (PVSC)*, pp. 394–399 (2009).
44. A. A. Maradudin, J. R. Sambles, and W. L. Barnes, *Modern Plasmonics*, Elsevier, Netherlands (2014).
45. S. A. Maier, *Plasmonics: Fundamentals and Applications*, Springer Science and Business Media LLC, New York (2007).
46. E. A. Freeman and G. G. Moisen, Elsevier, “A comparison of the performance of threshold criteria for binary classification in terms of predicted prevalence and kappa,” *Ecol. Modell.* **217**(1), 48–58 (2008).
47. W. Chen, R. L. Nelson, and Q. Zhan, “Geometrical phase and surface plasmon focusing with azimuthal polarization,” *Opt. Lett.* **37**(4), 581–583 (2012).
48. D. Choi et al., “Plasmonic optical interference,” *Nano Lett.* **14**(6), 3374–3381 (2014).

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