Chapter 1
OVERVIEW OF LITHOGRAPHY

The patterns of integrated circuits are created on wafers by lithography. The steps of this critical manufacturing process are listed in Table 1.1. Each step will be discussed at length in later chapters of this book, but a brief description of each will be given here. Most of this book is devoted to photolithography, where optical methods are used to transfer the circuit patterns from master images—called masks or reticles—to the wafers. Photolithography is the method used for patterning nearly all integrated circuits fabricated today.

Adhesion promotion: The lithography process creates the patterns of integrated circuits in films of specialized materials called resists, which are coated onto the wafers on which the circuits are made. Resists typically do not adhere properly to untreated surfaces of silicon or silicon-containing materials, such as silicon dioxide and silicon nitride. To ensure proper adhesion, the wafer surfaces are treated prior to resist coating.

Resist coat: Resists typically comprise organic polymers applied from a solution. To coat the wafers with resist, a small volume of the liquid resist is first dispensed onto a wafer. The wafer is then spun about its axis at a high rate of spin, flinging off the excess resist and leaving behind, as the solvent evaporates, a thin (0.1–2.0 μm, typically) film of solid resist.

Table 1.1 The steps in the lithography process. The steps in italic are optional.

Adhesion promotion
↓
Resist coat
↓
Softbake
↓
Alignment
↓
Exposure
↓
Post-exposure bake
↓
Development
↓
Hardbake
↓
Measurement and inspection

Softbake: After the resist coating has been applied, the density is often insufficient to support later processing. A bake is used to densify the resist film and drive off residual solvent.

Alignment: Integrated circuits are fabricated by a series of patterning steps. These start with a lithography operation followed by an etch or ion implantation. Between patterning steps, there may be film depositions, planarizations, and other processes. Each new pattern must be placed on top of preceding layers, and proper overlay of the new layer to the circuit pattern already on the wafer is achieved during the alignment step by using specialized equipment.

Exposure: Photoresists are materials that undergo photochemical reactions when exposed to light. There are two types of photoresists—positive and negative. Positive resists are normally insoluble in the chemicals referred to as resist developers, but are made soluble by exposure to light. Negative resists have the opposite behavior: they are soluble in developer and rendered insoluble by exposure. By exposing the resist selectively in some areas and not others, the pattern of the circuit can be created in the resist film. This selective exposure is accomplished in optical lithography by the imaging of a mask. Photomasks are sheets of glass, partially covered by an opaque material, usually chromium, that has been removed according to the pattern of the circuit. By shining light onto the mask, and then projecting the transmitted image onto the resist film, the pattern of one layer of the circuit is transferred to the resist film on the wafer.

Post-exposure bake: This is an optional baking step used to drive additional chemical reactions or the diffusion of components within the resist film. The purposes of the post-exposure bake are discussed in Chapters 3 and 4.

Development: This is the step by which a resist is removed, depending upon whether or not it has been exposed.

Measurement and inspection: This is an optional operation where it is determined by measurement if the resist features on the wafer are sized correctly and properly overlay preceding patterns, and that they are sufficiently free from defects. These measurements may be used for the purposes of process control or dispositioning.

Hardbake: This is another optional process. Because wafers with photoresist patterns nearly always go into etch or ion implantation operations immediately following the lithography step, a final bake is often used to drive out volatile organic materials and water in order to preserve the vacuum integrity of the etch and ion implantation equipment. The temperature required for this step is usually so high that it will degrade the photochemical properties of the resist. Had the high-temperature hardbake been employed prior to the development step, the resist would not have developed properly. Consequently, the hardbake is one of

the last steps in the lithography process, though it may precede measurement and inspection.

The role of the lithography process in overall integrated circuit fabrication can be appreciated by considering the sequence of deposition, lithography, and etch steps used to establish electrical contacts to the transistors that make up integrated circuits (Fig. 1.1). Electrical interconnections are made after the transistors have been fabricated and covered with insulating oxide or another suitable dielectric. The wafers are then covered with resist, and the resist is exposed in places where electrical contacts to the transistors are desired. For reasons explained later, positive resists are commonly used for making electrical contacts. The exposed resist is developed out, exposing the oxide above the points where electrical contact is desired. The wafer is then put into an environment of oxide etchant. The oxide still covered by resist is protected against the etch, while the oxide is removed where electrical contact is desired. The contact holes can then be filled with metal, thus establishing electrical contact.

The primary tool used for projecting the image of the circuit from a photomask onto a resist-coated wafer is the wafer stepper. Wafer steppers exist in two configurations—step-and-repeat and step-and-scan. In a step-and-repeat system, the wafer is positioned under a lens so that a projected image of the layer to be exposed will properly overlay the patterns already on the wafer (Fig. 1.2).

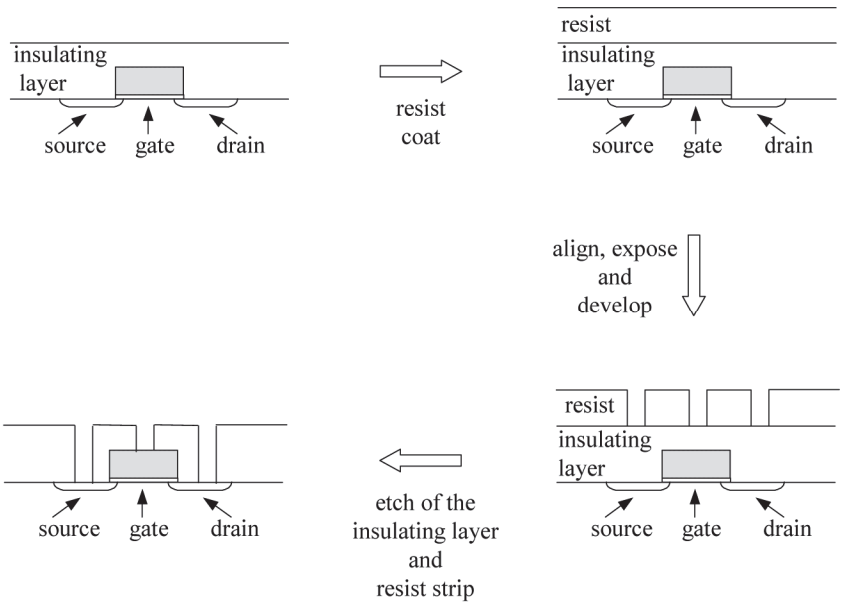


Figure 1.1 The sequence of steps used to make electrical connections in a planar transistor in an integrated circuit.

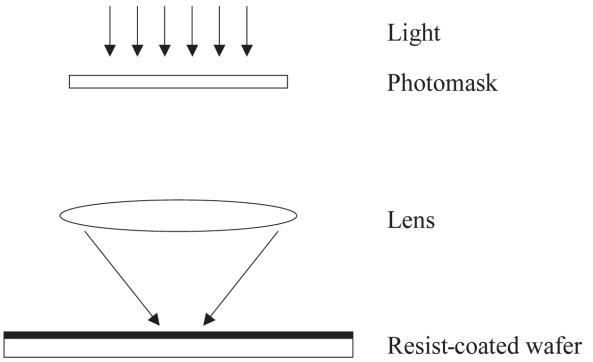


Figure 1.2 Exposure of resist-coated wafers on wafer steppers.

The systems that allow the stepper to bring the wafer into proper position are discussed in Chapter 6. Once the wafer is properly positioned and brought into focus, a shutter in an illumination system is opened, allowing light to pass through the photomask. The pattern on the mask is then imaged by the lens onto the wafer. The image is reduced laterally by the amount N:1, where N is the lens-reduction factor, most commonly equal to 4 in leading-edge systems today. Values of N of 1, 2, and 2.5 are found on steppers that have been designed primarily for high productivity.

Large values of N are desirable to the extent that they reduce the effects of variations in linewidths and misregistration on the reticle, generally by the factor of N, as the image of the reticle is projected onto the wafer. Defects are also reduced in size to the point that they often fall below the resolution limit of the lens. The first commercially available wafer stepper, the GCA DSW4800, had $N = 10$. However, as chip sizes became larger, smaller values of N were required to avoid reticles that were bigger than what was practical. For many years, most steppers had lens-reduction factors of 5, but values of 4 began to appear in the early 1990s. They are found on all leading-edge systems today. For a given mask size, larger exposure fields on the wafer are possible with smaller values of N, and systems designed for high productivity (but not necessarily to produce the finest patterns) often have $N < 4$. With larger exposure fields, fewer fields need to be exposed in order to pattern wafers completely, which gives an opportunity for higher throughput.

Because of reduction by the projection optics, only part of the wafer (an "exposure field") is exposed at any one time on a wafer stepper. After one field is exposed, the wafer is moved on an extremely precise stage so that another part of the wafer can be exposed. This process of exposure and wafer stepping is repeated until the entire wafer is exposed. In the typical reduction stepper, the stage travels in the horizontal plane beneath a fixed, vertically mounted lens.[*]

[*] The Micrascan systems on which wafers moved vertically were exceptions but are no longer being manufactured. These exposure tools were originally made by Perkin-Elmer. The Perkin–Elmer exposure tool business was purchased by SVG, Inc., which in turn was acquired by ASML.

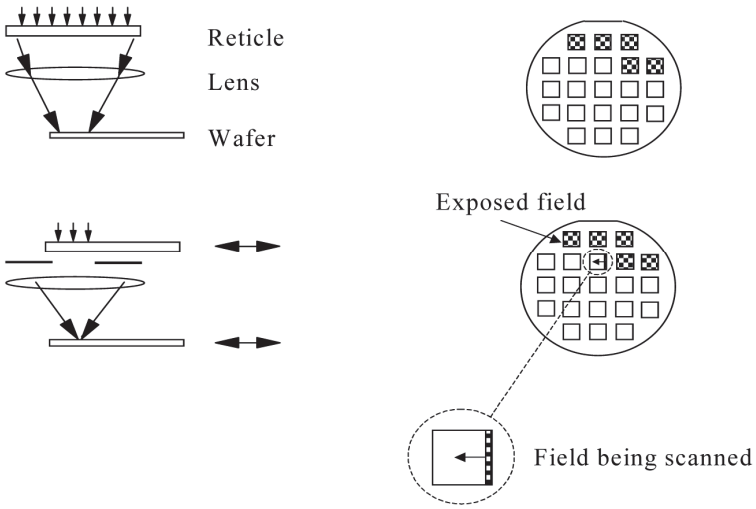


Figure 1.3 Step-and-repeat and step-and-scan configurations.

In a step-and-repeat system, the entire area of the reticle to be exposed is illuminated when the shutter is opened. In a step-and-scan system, only part of the reticle, and therefore only part of the exposure field on the wafer, is exposed when the shutter is opened (Fig. 1.3). The area exposed on step-and-scan systems at any instant is usually a narrow rectangular region, referred to as the slit. The entire field is exposed by scanning the reticle and wafer synchronously. The reticle stage must be scanned at a speed of N times faster than the wafer, where N is the lens-reduction factor. (The motivations for scanning are discussed in Chapter 5.)

This method of fabrication is extremely efficient, since many circuit features are patterned in parallel. For example, a NAND flash memory will have two contacts per bit in the memory arrays. With 34-nm design rules, four 32-Gb NAND flash memory chips are exposed simultaneously on a step-and-scan system when the mask is illuminated. Consequently, over 256 billion contacts are imaged in a single exposure, which occurs in about 0.1 sec. If one thinks of this in terms of a transfer of design information to the wafer, where each contact is considered to be a single piece of information, this is a remarkable rate of information transfer: over 2.5 *trillion* bits of information are transferred per second. Moreover, this rate of transfer continues to increase as lithography processes become able to print smaller features. This increasing rate of transfer, driven by the ability to print features of decreasing size, is the key factor in the reduction of the cost of microelectronics.

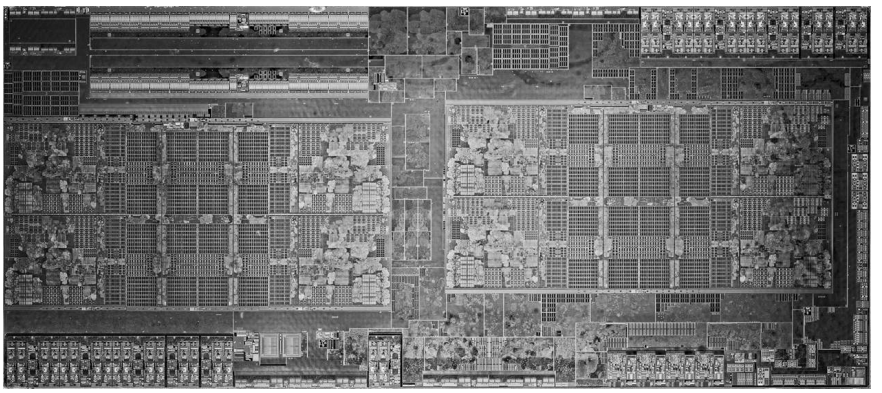
Each step of the lithographic process is discussed in this book. Pattern formation is of central importance because the great functionality of modern microelectronics has been enabled by the ability to pack large numbers of individual transistors in a unit area of silicon. The principles of optics relevant to imaging small features are covered in Chapter 2, while photoresists are discussed

in Chapter 3. Methods of predicting lithographic performance are presented in Chapter 4. The primary tool used in lithography—the wafer stepper—is described in Chapter 5, and this leads into overlay, the topic of Chapter 6. Mask technology is the subject of Chapter 7. Advanced methods of optical lithography are reviewed in Chapter 8. The problem of measuring the small features created by the lithography process is addressed in Chapter 9. The limitations imposed by the laws of physics on optical methods are discussed in Chapter 10. Lithography costs, which can be as significant as technical issues, are covered in Chapter 11. Finally, possible next-generation lithography options that might succeed optical lithography are reviewed in Chapters 12 and 13.

Problems

1.1 For a mask that is 152 × 152 mm, and assuming that a 10-mm border at the edges of the plate is required to hold the mask, show that the largest field that can be patterned on the wafer is 13.2 × 13.2 mm if the lens-reduction factor is 10×. What is the largest field if the factor is 5×? 4×?

1.2 The area of the AMD Ryzen microprocessor is 213 mm^2 (22 × 9.7 mm):



Can such a die be printed in a single exposure with an exposure tool with 10× lens reduction? 4× lens reduction? Why do you think that large lens-reduction factors are not used, even though their use would reduce the criticality of reticle quality?

1.3 What are the nine principal steps in the lithographic process? Which steps are optional?

1.4 In the lithographic process, what are the materials called in which patterns are formed on the wafers?